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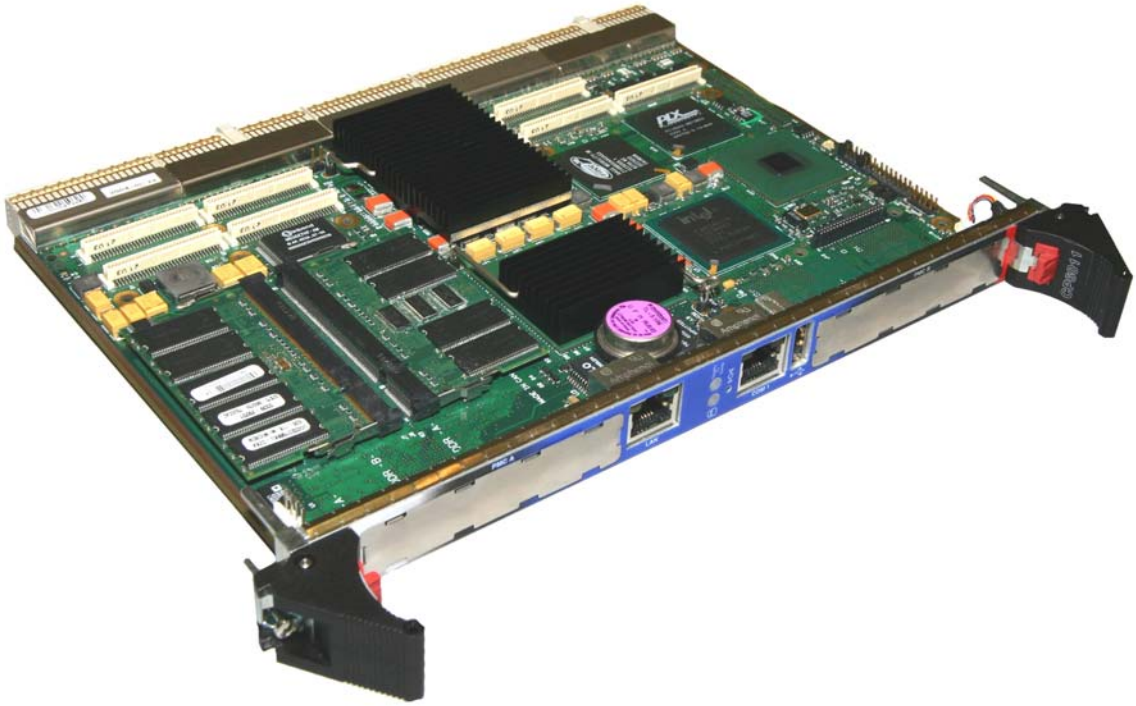
CP6011 User's Guide

Pentium-M

Document Revision 1.3



kontron

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A. Memory & I/O Maps

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C. Kontron Extension Registers

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Safety Instructions

Contents

Before You Begin

Before handling the board, read the instructions and safety guidelines on the following pages to prevent damage to the product and to ensure your own personal safety. Refer to the "Advisories" section in the Preface for advisory conventions used in this user's guide, including the distinction between Warnings, Cautions, Important Notes, and Notes.

- Always use caution when handling/operating the computer. Only qualified, experienced, authorized electronics service personnel should access the interior of the computer. The power supplies produce high voltages and energy hazards, which can cause bodily harm.

- Use extreme caution when installing or removing components. Refer to the installation instructions in this user's guide for precautions and procedures. If you have any questions, please contact Kontron Technical Support.

WARNING

High voltages are present inside the chassis when the unit's power cord is plugged into an electrical outlet. Turn off system power, turn off the power supply, and then disconnect the power cord from its source before removing the chassis cover. Turning off the system power switch does not remove power to components.

When Working Inside a Computer

Before taking covers off a computer, perform the following steps:

Turn off the computer and any peripherals.

Disconnect the computer and peripherals from power sources or subsystems to prevent electric shock or systemboard damage. This does not apply to when hot-swapping parts.

Follow the guidelines provided in “Preventing Electrostatic Discharge“ on the following page.

Disconnect telephone or telecommunications lines from the computer.

In addition, take note of these safety guidelines when appropriate:

- To help avoid possible damage to system boards, wait five seconds after turning off the computer before removing a component, removing a system board, or disconnecting a peripheral device from the computer.

- When you disconnect a cable, pull on its connector or on its strain-relief loop, not on the cable itself. Some cables have a connector with locking tabs. If you are disconnecting this type of cable, press in on the locking tabs before disconnecting the cable. As you pull connectors apart, keep them evenly aligned to avoid bending any connector pins. Also, before connecting a cable, make sue both connectors are correctly oriented and aligned.

CAUTION

Do not attempt to service the system yourself, except as explained in this user’s guide. Follow installation and troubleshooting instructions closely.

Preventing Electrostatic Discharge

Static electricity can harm system boards. Perform service at an ESD workstation and follow proper ESD procedure to reduce the risk of damage to components. Kontron strongly encourages you to follow proper ESD procedure, which can include wrist straps and smocks, when servicing equipment.

Take the following steps to prevent damage from electrostatic discharge (ESD):

- When unpacking a static-sensitive component from its shipping carton, do not remove the component's antistatic packing material until you are ready to install the component in a computer. Just before unwrapping the antistatic packaging, be sure you are at an ESD workstation or grounded. This will discharge any static electricity that may have built up in your body.

- When transporting a sensitive component, first place it in an antistatic container or packaging.

- Handle all sensitive components at an ESD workstation. If possible, use antistatic floor pads and workbench pads.

- Handle components and boards with care. Don't touch the components or contacts on a board. Hold a board by its edges or by its metal mounting bracket.

- Do not handle or store system boards near strong electrostatic, electromagnetic, magnetic, or radioactive fields.

Working with Batteries

Care and Handling Precautions for Lithium Batteries

Your computer board has a standard, nonrechargeable lithium battery.

Do not short circuit

- Do not heat or incinerate
- Do not charge
- Do not deform or disassemble
- Do not apply solder directly
- Do not mix different types or partially used batteries together
- Always observe proper polarities

Replacing Lithium Batteries

Exercise caution while replacing lithium batteries!

WARNING

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries, following manufacturer's instructions.

ATTENTION

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabriquant.

ACHTUNG

Explosionsgefahr bei falschem Batteriewechsel. Verwenden Sie nur die empfohlenen Batterietypen des Herstellers. Entsorgen Sie die verbrauchten Batterien laut Gebrauchsanweisung des Herstellers.

ATENCION

Puede explotar si la pila no este bien reemplazada. Solo reemplazca la pila con tipas equivalentes segun las instrucciones del manifacturo. Vote las pilas usads segun las instrucciones del manifacturo.

Preface

Contents

How to Use This Guide

This user's guide is designed to be used as step-by-step instructions for installation, and as a reference for operation, troubleshooting, and upgrades.

You can find the latest release of this User's Guide at:
http://www.kontron.com or at: ftp://ftp.kontron.ca/support/

For the circuits, descriptions and tables indicated, Kontron assumes no responsibility as far as patents or other rights of third parties are concerned.

The following is a summary of chapter contents:

- Chapter 1, Product Description
- Chapter 2, Onboard Features
- Chapter 3, Installing the board
- Chapter 4, Building a CPCI System
- Chapter 5, Software Setup
- Appendix A, Memory & I/O Maps
- Appendix B, Interrupt Lines
- Appendix C Kontron Extension Registers
- Appendix D, Board Diagrams
- Appendix E, Connector Pinout
- Appendix F, BIOS Setup Error Codes
- Appendix G, BIOS Update & Emergency Procedure
- Appendix H, Getting Help

Customer Comments

If you have any difficulties using this user's guide, discover an error, or just want to provide some feedback, please send a message to: Tech.Writer@ca.kontron.com. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user's guide in our Web site. Thank you.

Advisory Conventions

Seven types of advisories are used throughout the user guides to provide helpful information or to alert you to the potential for hardware damage or personal injury. They are Note, Signal Paths, Related Jumpers, BIOS Settings, Software Usage, Cautions, and Warnings. The following is an example of each type of advisory. Use caution when servicing electrical components.

Note :
Indicate information that is important for you to know

Signal Paths:
Indicate the places where you can fin the signal on the board

Related Jumpers:
Indicate the jumpers that are related to this sections

BIOS Settings :
Indicate where you can set this option in the BIOS

Software Usage :
Indicates how you can access this feature through software.

CAUTION

Indicate potential damage to hardware and tells you how to avoid the problem.

WARNING

Indicates potential for bodily harm and tells you how to avoid the problem.

Disclaimer: We have tried to identify all situations that may pose a warning or a caution condition in this user's guide. However, Kontron does not claim to have covered all situations that might require the use of a Caution or a Warning.

Unpacking

Follow these recommendations while unpacking:

- Remove all items from the box. If any items listed on the purchase order are missing, notify Kontron customer service immediately.
- Inspect the product for damage. If there is damage, notify Kontron customer service immediately.
- Save the box and packing material for possible future shipment.

Powering Up the System

Before any installation or setup, ensure that the board is unplugged from power sources or subsystems.
If you encounter a problem, verify the following items:

- Make sure that all connectors are properly connected.
- Verify your boot devices.
- If the system does not start properly, try booting without any other I/O peripherals attached, including Compact PCI or PMC adapters.

If you still cannot start your system, please refer to the Emergency Procedure in the Appendix Section of this User's Guide.

Make sure your system provides the minimum DC voltages required at the board's slot, especially if DC power is carried by cables.

If you are still not able to get your board running, contact our Technical Support for assistance.

Adapter Cables

Because adapter cables come from various manufacturers, pinouts can differ. The direct crimp design offered by Kontron allows the simplest cable assembly. All cables are available from Kontron Sales Department.

Storing Boards

Electronic boards are sensitive devices. Do not handle or store device near strong electrostatic, electromagnetic, magnetic or radioactive fields.

Regulatory Compliance Statements

This section provides the FCC compliance statement for Class B devices and describes how to keep the system CE compliant.

FCC Compliance Statement for Class B Devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generated, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experience radio/TV technician for help.

WARNING

This is a Class B product. If not installed in a properly shielded enclosure and used in accordance with this User's Guide, this product may cause radio interference in which case users may need to take additional measures at their own expense.

UL Certification

This product bears the combined UL Recognized Component Mark for Canada and U.S. It indicates investigations to the UL Standard for Safety of Information Technology Equipment, Including Electrical Business Equipment. It is destinated to be used in end-product equipment where the acceptability of the combination is determined by Underwriters Laboratories Inc.

CE Certification

The product(s) described in this user's guide complies with all applicable European Union (CE) directives if it has a CE marking. The CE declaration of conformity is provided on the last page of this user's guide. For computer systems to remain CE compliant, only CE-compliant parts may be used. Maintaining CE compliance also requires proper cable and cabling techniques. Although Kontron offers accessories, the customer must ensure that these products are installed with proper shielding to maintain CE compliance. Kontron does not offer engineering services for designing cabling systems. In addition, Kontron will not retest or recertify systems or components that have been reconfigured by customers.

Limited Warranty

Kontron Canada, Inc, ("The seller") warrants its boards to be free from defects in material and workmanship for a period of two (2) years commencing on the date of shipment. The liability of the seller shall be limited to replacing or repairing, at the seller's option, any defective units. Equipment or parts, which have been subject to abuse, misuse, accident, alteration, neglect, or unauthorized repair are not covered by this warranty. This warranty is in lieu of all other warranties expressed or implied.

1. Product Description

Contents

1.1 Product Overview

The CP6011 is without a doubt the most powerful CompactPCI CPU engine you can get in a single slot (4HP). Its use of the Intel Pentium-M (and Low Voltage Pentium-M) processors at 1.6GHz, 1.8GHz and at 2.0GHz (and 1.1GHz) and future speeds when they become available guarantees performance and high density. The low power features of the Pentium-M processor make it possible to fit in a single slot and therefore potentially double overall system density. Combined with a high I/O throughput chipset like Intel's E7501 and up to 2GB of DDR memory distributed over two separate channels for increased memory bandwidth, this board is designed to meet the requirements of the most demanding applications. The CP6011 has two SODIMM sockets (with Registered / ECC support) for a better combination of flexibility, capacity and cost efficiency.

Finding the product that exactly matches all application requirements can be a difficult task. Kontron, however, made it easier by offering the CP6011 with two PMC slots that can be populated with Kontron or third party products. The wide acceptance of the PMC standard and the availability of several different flavors of PMC will allow customers to easily tailor the CP6011 to their requirements in a very short amount of time. The first high performance PMC slot (up to 64-bit/133MHz PCI-X) also supports the PMC I/O Module (PIM) standard, thus allowing the access of the PMC I/O signals on Kontron's rear transition module (RTM). The second PMC slot has an interface that can reach up to PCI-X 64-bit/100MHz.

The CP6011 has Dual Gigabit Ethernet 2.16-compliant ports and a third 100Base-T Ethernet port on the front panel for management or other purposes. Additional Gigabit Ethernet ports and Ultra160/320 SCSI can be added through Kontron PMC cards (respectively PMC240 and PMC261). CP6011 also has VGA support through the use of ATI's Mobility-M graphics chip. It also features CompactFlash support, ATA/100 and programmable user LED's for software use.

The CP6011 is capable of driving a cPCI bus segment that can scale from 32-bit/33MHz to 64-bit/133MHz PCI-X. Since the chipset has two independent 64-bit/133MHz PCI-X buses, it ensures that a board driving an external bus, two PMC's and the dual Gigabit Ethernet, will maintain a high level of performance.

In today's systems, whether they are in communications, medical or industrial environments, serviceability is critical and the ability to manage an entire system remotely is often an obligation. The groundwork for such an environment is the Intelligent Platform Management Interface (IPMI). The CP6011 includes a Baseboard Management Controller (BMC) that incorporates Kontron's IPMI firmware, which allows the board to act as an IPMI BMC or as a satellite in one of Kontron's High Availability platforms. Kontron's Xtreamlink family of system products includes two platforms with such management capabilities; the XL-VHDS (10U carrier class platform) and the XL-LP42 (4U low profile platform).

As a powerful, very flexible and high density CPU engine, the CP6011 is intended for applications calling for distributed high processing capabilities and tremendous I/O throughput. Those are likely to be VoIP applications (Softswitch, Media Gateway, Signalling Gateway, trunking, call centers and IVR), wireless infrastructure applications (Base Stations Controller/RNC, SGSN/GGSN, SCP, HLR/VLR, billing, and wireless access gateway), datacom applications (database management, routing devices), medical applications (diagnosis) as well as industrial and military applications.

1.2 What's Included

This board is shipped with the following items:

1. One Quick Reference Sheet.
2. One CD-ROM containing drivers.
3. One CP6011 board
4. Cables that have been ordered

If any item is missing or damaged, contact the supplier.

1.3 Board Specifications

FEATURES	DESCRIPTION
Supported Microprocessors	• Single Pentium M® Processor at 400 / 533 MHz front side bus (FSB) up to 2.0GHz (and future speeds as they become available) • Passive heatsink
Cache Memory	• 1M L2 on-die cache (1.6GHz) • 2M L2 on-die cache (1.8GHz, 2.0GHz)
Chipset	• Intel E7501 MCH and south bridge Intel's ICH3-S • Front Side Bus: 400 / 533 MHz, 64-bit • Large I/O bandwidth: Two 64-bit/133MHz PCI-X bus plus one 32-bit/33MHz bus
Bus Interface	• Front side bus at 400 / 533 MHz, 64-bit data, 32-bit address • Memory bus at 200 /266 MHz, 144-bit data (2 channel) • Two onboard 64-bit/133MHz PCI-X bus • CPCI PCI-X 64-bit/133MHz with universal bridge 3.3V or 5V are available. (see available options) • One onboard 32-bit/33MHz bus for video interface and LAN management port • PCI-X 64-bit/133MHz with universal bridge (board can operate and access the cPCI in a system slot or peripheral slot or be isolated from the cPCI bus in any slot –drone mode-)
PMC Slot	• Slot A : Up to 64-bit/133MHz PCI-X • Slot B : Up to 64-bit/100MHz PCI-X • PMC I/O module (PIM) support through J4
System Memory	• Up to 2GB on 2 x 200-pin latching SO-DIMM sockets (1.45 inch maximum height) • Two DDR channels 72-bit 200/266MHz for Interleave operation • PC-1600/PC-2100 DDR, registered SDRAM non-ECC/ECC mode (ECC error correction up to a nibble, error detection for more than a nibble)
Flash Memory	• 1MB BIOS (field upgradeable with BIOS mezzanine and with PH FLASH software)

Board Specifications (continued)

I/O

Description	Front Plate	Rear I/O	Mezzanine	Total
Video	-	1	-	1
USB	1	2	-	3
Serial	1	2	-	2
PS/2 Mouse	-	1	-	1
PS/2 Keyboard	-	1	-	1
Ethernet (F / R)	1	2	2*	5
Hard Disk	-	2	1*	3
SCSI (optional)	-	-	2*	2
Compact Flash	-	-	1*	1
Floppy	-	1	-	1
Reset Button	1	-	-	1

* Various combinations of mezzanine options are possible

F / R	Front or Rear
Video	PCI video controller (ATI Mobility-M) with 4MB video memory. Support CRT with resolution up to 1600 x 1200, 65K colors
USB	USB 1.1 compliant
Serial	COM1 (RS232), COM2 (configurable as RS-232/RS-422/485)
Ethernet	10 Base-T/100 Base (Intel82551er) on faceplate and Two 10 Base-T/100 Base/1000 Base-T (Intel 82544GC) on rear I/O optional Gigabit Ethernet ports available on PMC
Hard Disk	PCI EIDE Ultra DMA/100, Rear I/O: Channel 1 Onboard: Channel 0
SCSI	Dual Channel Ultra 160/320 SCSI, LVD/SE based on LSI 53C10XXX using PMC
CompactFlash	Can be installed on EIDE channel 0 through the onboard connector

Clock/Calendar	• Real-time clock with 256-byte battery backup CMOS RAM
Connectors in Front configuration	**Front Plate** COM1 1 x RJ-45 (Serial Port) Ethernet 1 x RJ-45 (Ethernet) USB(1) 1 x 4-pin USB female *Optional SCSI PMC adapter with front connector
Interfaces on J3/J4/J5	**Rear CPCI I/O Connectors (J3/J4/J5)** **(Rear-panel transition module, cTM80-2 available separately)** CRT Serial Ports (2) USB (2) Speaker I/F Reset Switch Ethernet (2) PS/2 Mouse &Keyboard SCSI (with PMC) EIDE Floppy disk
Onboard Expansions	2 PCI Mezzanine Card PMC. CompactFlash. 4HP IDE Mezzanine

Board Specifications (continued)

BIOS Features	• Phoenix BIOS in Boot Block Flash with recovery code • Save CMOS in Flash option • Boot from LAN and from USB capability • Auto configuration, extended setup and VGA disable by jumper • Diskless, keyboard less, and video less operation extensions • System, video and LAN BIOS shadowing • Programmable memory wait states • HDD S.M.A.R.T. support • Advanced Configuration and Power Interface (ACPI 1.0), Intelligent System Monitoring (advanced thermal management such as resume, overheat alarm and auto slow down) • Setup console redirection to serial port (VT100 mode) with CMOS setup access
Supervisory	• Support a system management interface via an IPMI V1.5 compliant controller • Two-stage software programmable watchdog timer, time out from 16msec to 4.5min with history. • Silicon Serial ID TAG for unique board identification accessible via software • Hardware system monitor (voltages, temperature), CPU temperature monitor / alarm; board temperature sensor, power failure / low battery detector; SMBus • Current monitoring using IPMI
OS Compatibility	• Microsoft Windows 2000 family • Microsoft Windows XP • Microsoft Windows Server 2003 • Linux Fedora Core 3 • FreeBSD 5.2 • And other OSs
Hardware Compatibility	• Upgrade path for many previous Kontron's boards (MXS64, MXP64, MXS64GX, MXP64GX) • CPCI J3, J4 and J5 pinouts is the same as the DT64 and the CP6010 but has been changed from previous boards. **Do not use older Rear Transition Modules (RTMs) with this board.** **Use only the CTM80-2 RTM or contact technical support for other RTM availability.**
Mechanical	• 6U (10.5") x 6.3" x 4HP, Standard cPCI 6U board
Power Requirements	Supply Voltage Vcc = +3.3V +5% -3% +5V +5% -3% +12V ± 5% +12V ± 5%

	2.0G, 2Gig DDR	1.8G, 2Gig DDR	1.6G, 2Gig DDR	1.1G, 2Gig DDR
ICC +5V	8.8 A max.	5.6 A max.	7.4 A max.	3.4 A max.
ICC +3.3V	4.2 A max.	6.1 A max.	5.9 A max.	5.9 A max.
ICC +12V	0.3 A max.	0.3 A max.	0.3 A max.	0.3 A max.
ICC –12V	< 10 mA max.	< 10 mA max.	< 10 mA max.	< 10 mA max.
Power Max :	61.2 W	52 W	60 W	40 W

Mesured with MaxPower and Memtest 2.0

Board Specifications (continued)

Environmental		Operating	Storage and Transit
	Temperature	0-55°C/32-131°F	-40 to +70°C/-40 to 158°F
	Air Flow	Consult table below	
	Humidity	5% to 90% @40°C/104°F non-condensing	5% to 95% @ 40°C/104°F non-condensing
	Altitude*	4,000 m / 13,123 ft	15,000 m / 49,212 ft
	Shock	30G, half-sine 11ms, each axis	Bellcore GR-63-CORE Section 4.3
	Vibration	1.0G, 5-500Hz each axis	2.0G, 5-50Hz; 3.0G, 50-500Hz each axis
Reliability	• MTBF: > 134 000 hours @ 25°C / 77°F (Telcordia SR-332, Issue 1) • Whole board protected by active breaker • USB voltage protected by an active breaker • Mouse / keyboard voltage protected by self-resetting fuses		
Safety/EMC	Meet or exceed: • Safety: UL 60950 3rd Ed.; CSA C22.2 No 60950-00; EN 60950:2000; IEC60950-1 • EMI/EMC: FCC 47 CFR Part 15, Class B; CE Mark to EN55022/EN55024		
Warranty	Two year limited warranty		

* Designed to meet or exceed

Airflow*

Configuration	Max. Ambient °C	CFM	LFM
Base board	40**	7.5**	200**
	55**	16.24**	422**
PMC Ethernet and PMC SCSI	36**	7.5**	200**
	55**	21.7**	471**

* For more configurations, please call Technical Support.
** These results are shown for reference only and might differ from your system and CPUs.

1.4 Compact PCI Compliance

This product conforms to the following specifications:

- PICMG2.0R3.0 (core specification)
- PICMG2.1R2.0 (hot swap specification)
- PICMG2.9R1.0 (system management)
- PICMG2.10R1.0 (keying of CPCI boards)
- PICMG2.16R1.0 (packet switching)

1.5 Hot-Swap Capability

The CP6011 supports **Full Hot Swap** capability as per PICMG2.1R2.0. The T6011 can be removed from or installed in the system while it is on (without powering-down the system). Please refer to the PICMG2.1R2.0 specification for additional details. The following paragraphs describe some of the most important features of the hot swap system.

1.5.1 Board Level:

You may encounter these types of boards:

Type of board	Description
Non hot swap	The board has none of the features required for hot swap. It is not electrically safe to hot swap a board in a powered system.
Basic hot swap	The board has the minimum feature set to allow electrically safe insertion in a live system. It is up to the system operator to use and configure the board after it is inserted.
Full hot swap	In addition to the basic hot swap feature, there are additional provisions for automatic software control over the connection process. This gives the broadest range of system capability. Boards in this class provide the following signals: ENUM#, BDSEL#, HEALTHY#. Full hot swap boards also provide a blue LED and a switch in the lower ejector for interaction with the operator.

1.5.2 System Level:

At this level, hot swap capability depends on the boards and on the chassis.

Type of board	Description
Non hot swap	There is not any hot swap capability in this class of system; live insertion of any type of board is unsafe.
Basic hot swap	It is electrically safe to insert a basic or full hot swap board in the chassis. However, the operator must do the software connection process.
Full hot swap	This adds automatic software connection process to the basic hot swap model. A signal (ENUM#) is used to notify the system slot when a peripheral board is newly inserted or when a board is about to be extracted.
High availability	This is strictly system dependent. A full hot swap board already meets the electrical requirement for a High Availability system, but the system itself may fall in the Full Hot Swap category if it is not controlling the hardware connection process. In addition to the automatic software connection process, a High Availability system adds more control over the hardware such as reset and power control of each slot of the system.

The following signals are used:

BDSEL#: This is a short pin. It is the last to mate or the first to break contact. This signal allows the system to detect the presence of a board and also to control its power state. Systems other than High Availability have this pin grounded.

HEALTHY#: This is a normal length pin. Peripheral boards are required to drive this signal low when they are ready to join the PCI bus. This signal will not be asserted when the current operating mode of the bus is not compatible or when the back end power is not good or for any other reason.

PCIRST#: This signal resets the PCI bus when driven low. High availability can implement this signal as a radial signal from the Hot Swap Controller (HSC) to further control the electrical connection. Platforms that do this must OR the system host's reset signal with the slot-specific signal to maintain the bused signal's function.

M66EN: On a High Availability platform compatible with R. 2.0 of PICMG2.1, the signal may be radial from the HSC. This allows the platform to accept 33MHz only peripheral boards that comply with R. 1 of the specification.

Note:
Hot Swap of the system slot is not defined in the PICMG2.1R2.0 specification. It is electrically possible to hot swap the CP6011 in a system slot, but system functionality is lost and the PCI bus will float.

WARNING

It can be harmful for some PCI peripheral devices to remove system slots because the PCI bus floats. At least PCIRST# should be asserted but not all platforms detect this condition and hold the system in reset when a system board is not present. Please consult your chassis manual.

1.5.3 Hot swap compatibility with Kontron's systems:

	XL-VHDS	XL-PSB	XL-CXP	XL-LP41	XL-LP42
CP6011	High availability (1)	Full hot swap	CP6011 is not supported in this chassis	High availability (2)	High availability (2)

1) When system management card used.

2) No supported for radial RESET# and radial M66EN.

1.5.4 Full hot swap mechanism

Full Hot Swap boards such as the CP6011 in peripheral mode drive the ENUM# signals to the system host to indicate a service request. This signal notifies the system host that either a board has been inserted or is about to be extracted and that the configuration of the system has or will change. Then, the system host performs maintenance such as assigning resources to PCI devices or installing or removing a device driver and any other task. Some of the above functionalities may be implemented in the OS; others may need specific application software. More details on Hot Swap can be found on the PICMG 2.12 specification.
The Hot Swap Switch is in the lower ejector. It allows the operator to inform the system about the intention to extract the board. A blue LED, located on the board's faceplate, illuminates when it is safe to extract the board. This LED indicates that the system software has been placed in a state for orderly extraction of a board. The hardware connection layer provides protection only for the hardware during insertions and extractions. This method allows the operator to insert or to extract boards without reconfiguring the system with the console.

Note:
In order to detect handle switch activity and to signal board status with the blue LED, a proper hot swap driver must be running on the host.

End user must be aware that adding PCI device in a live system require PCI ressources allocation. This is not done by the OS. It has to be done by a hot swap driver. Consult Kontron's technical support if you need doing that.

WARNING

All actions are initiated by the operator, and must be performed in the correct sequence for proper system operation.

Full Hot Swap boards present the following resources to software executing on the system host (nominally implementing the Hot-Plug Service and Hot-Plug System Driver)

- An ENUM# signal, which is an open collector (open drain) bussed signal, to signal a change in status for the board.
- A switch actuated with the lower ejector handle, indicating the beginning of the extraction process or end of the insertion process.
- A LED to indicate the status of the software connection process.
- A set of four control and status bits (hot swap register in PCI configuration space) on each board allows the system host's software to determine the source of the ENUM# signal and control the LED.

1.5.5 High Availability mechanism

When using High Availability system such as XL-VHDS and XL-LP42, the system has more control over the hardware connection process compared with the full hot swap model. When a board is inserted in the system, the Hot Swap Controller (HSC) detects this insertion before powering up the newly inserted board. When the HSC is ready to power up a card, it asserts BDSEL# and monitor the HEALTHY# signal for that card. This flexibility gives the possibility to the operator, for example, to cycle the power state of a problematic I/O board or to reset only a particular slot. Refer to your system manual for more details on how to use the High Availability feature of the system.
In addition to the resources a board present to Full Hot Swap system, the following ones are usable on HA systems:

- A BDSEL# signal controls the power state of the board
- A HEALTHY# signal indicates the healthiness of the board

1.5.5.1 Bus less operation

When the onboard bridge is disabled, the CP6011 is considered bus less. In such case, the SBC can be hot swapped in a CPCI bus but will not try to participate on the bus. Then, BDSEL# and HEATHY# preserve their functionality but PCIRST# is ignored. The "blue led" mechanism from the bridge is disabled since the onboard bridge and system host can't handle it. However, it is possible to read the handle switch and control the blue LED through the register 0x192.

Note:
When bridge is disabled (Stand alone operation), user can read the hot swap switch and drive blue LED using register 0x192. The BMC can overwrite this register.

1.6 Interfacing with the Environment

1.6.1 CPCI

The CP6011 system/peripheral processor board is provided for rack-mounted systems to offer the highest modularity. Through the J1/J2 segment, the board can drive up to **seven** external CompactPCI slots, supporting individual REQ/GNT arbitration pair signals and the clock.
The CP6011 supports all PCI and PCI-X modes for operation up to 133MHz, giving a theoretical throughput of 1GB/s.
Possible PCI modes of the CP6011 with Kontron systems:

	XL-VHDS (1)	XL-PSB	XL-LP41	XL-LP42
CP6011	PCI-33 PCI-66 PCIX-66 PCIX-100	PCI-33	PCI-33	PCI-33 PCI-66

1) Using a five-slot backplane. Call technical support for 133MHz backplane availability.

1.6.2 RTM (rear transition module)

All I/O can be accessed through the use of a RTM. RTM use a proprietary pinout in J3/J4/J5 to bring out all I/O of the SBC. Only use Kontron's RTM with the CP6011. Currently compatible RTM is the cTM80-2.
RTM are not designed to be hot swapped. Always make sure that either the system is shut off or that the front board of the RTM is unpowered before removing or installing the RTM.

Note:

A. **In front I/O configuration**, the following I/Os signals are available on the faceplate: Serial Port COM1 (RJ-45), USB Port 1, Ethernet 1. All other I/Os are connected to J3, J4, and J5.

B. **In Rear I/O configuration**, all I/O signals are connected to J3, J4 and J5

1.6.3 Mezzanine

The mezzanine is a hardware interface used to increase I/O connectivity of the CP6011 while respecting the single slot 4HP form-factor restrictions. It is built around three sets of connectors:

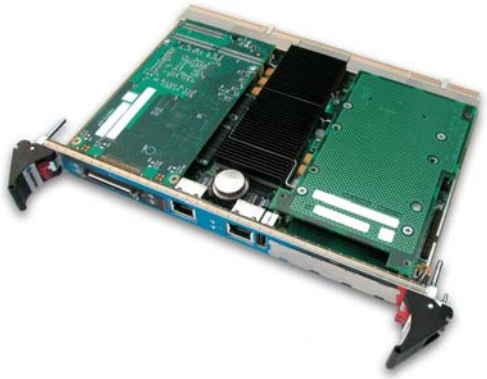
- Mezzanine connector handling IDE signals.
- PMC A Mezzanine connectors (4) that handle an independant PCIX signal set, including the REQ/GNT arbitration signal pair. (64bits/133MHz) And the PIM interface
- PMC B Mezzanine connectors that handles a complete PCIX signal set, including the REQ/GNT arbitration signal pair. This PCI channel is bussed with the 2 Gig Ethernet and the Bridge.(64bits/100MHz)
- CompactFlash Mezzanine connector that handle all the signals to connect a CompactFlash Module.
- These connectors represent an open door for future development of expansion and I/O mezzanine cards. The IDE support is used with the T6508 mezzanine.

See Kontron's mezzanine offering for additional I/O capabilities.

1.6.3.1 PMC Expansion

The mezzanine increases the I/O capability of the CP6011 by providing two PMC slots. Up to 133MHZ/64-bits are supported for up to 1GB of I/O bandwidth.

The capability of the CP6011 to connect with other devices is enforced by PCI Mezzanine Cards (PMC). A CP6011 equipped with a SCSI PMC and a T6508 mezzanine board may appear as follows:



1.7 Compatibility with Kontron Products

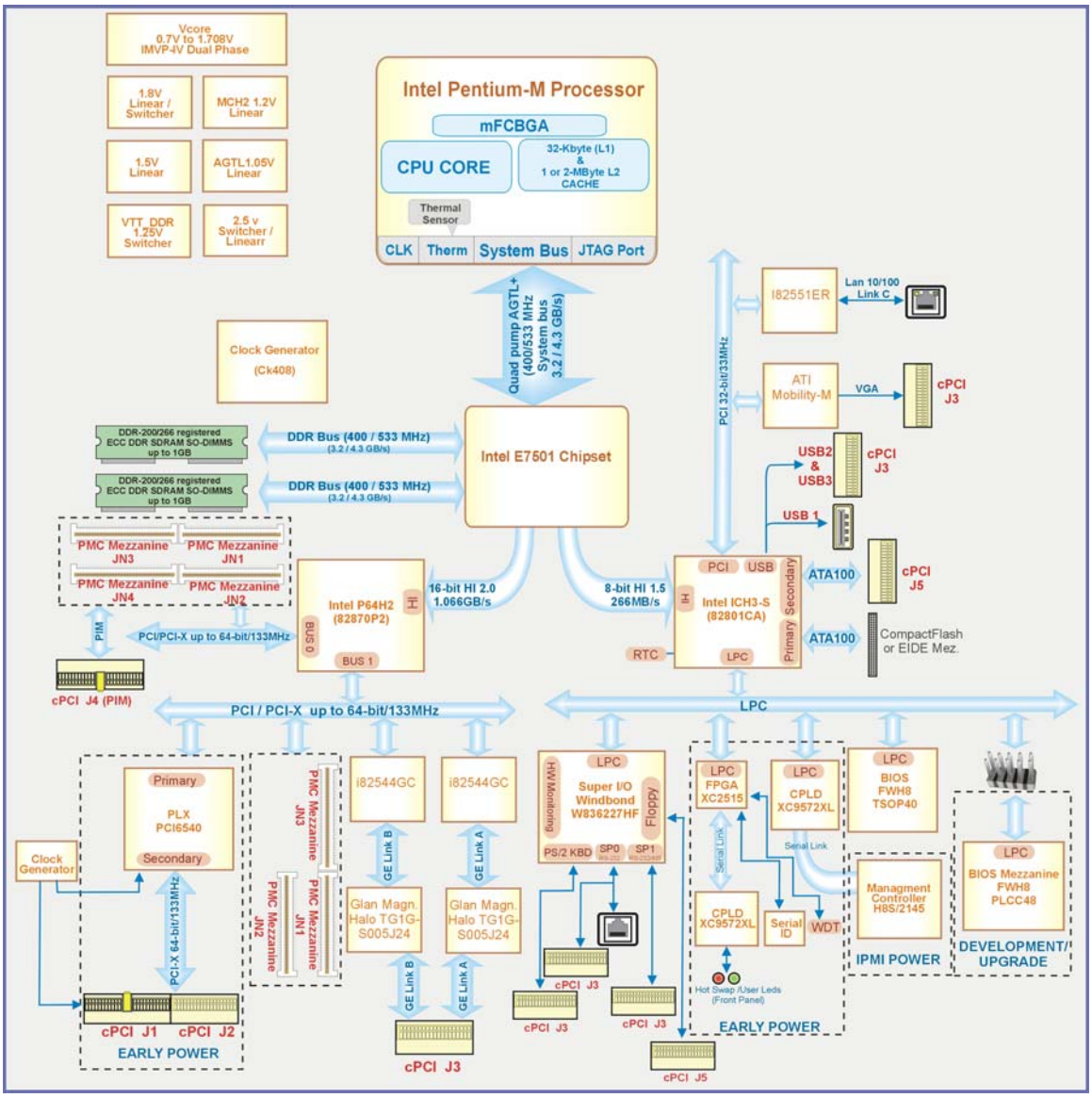
The CP6011 system processor is a member of Kontron's CompactPCI product family.
When building a basic environment around the CP6011, the platform can be composed of any of the following devices:

XL-VHDS	• CP6011 6U system board (up to 17), including other Kontron cPCI SBCs • CTM80-2 6Ux8HPx80mm RTM (for CP6011) • Third party CPCI I/O board with RTM as needed • Storage module with 2.5-inch hard disk and DVD or floppy • Up to 12 hot swappable SCSI drives • Up to six 3U 250W power supply • Up to two Ethernet switches (PICMG2.16) • Up to two PMM (Platform management module) • AC or DC (redundant –48 volts) power input
XL-PSB	• CP6011 6U system board (up to 12), including other Kontron cPCI SBC • CTM80-2 6Ux8HPx80mm Rear Transition Module (for CP6011) • Third party CPCI I/O board with RTM as needed • Up to two 6U 350W power supplies • Two Ethernet switches (PICMG2.16) • AC power input
XL-LP41	• One 7-slot PCI segment + one 2.16 Fabric slot • CP6011 6U system board (up to 7), including other Kontron cPCI SBCs • CTM80-2 6Ux8HPx80mm RTM (for CP6011) • Third party CPCI I/O board with RTM as needed • Up to three 3U 250W power supplies • One Ethernet switche (PICMG2.16) • One optional CMM (Chassis Management Module) • AC or DC power input
XL-LP42	• Two PCI segments (4 slots + 3 slots) + One 2.16 Fabric slot • CP6011 6U system board (up to 7), including other Kontron cPCI SBCs • CTM80-2 6Ux8HPx80mm RTM (for CP6011) • Third party CPCI I/O board with RTM as needed • Up to three 3U 250W power supplies • One Ethernet switche (PICMG2.16) • One CMM (Chassis Management Module) • AC or DC power input

2. Onboard Features

Contents

2.1 Block Diagram



2.2 System Core

2.2.1 Processors

The Intel® Pentium® M processor is a high performance, low power mobile processor with several micro-architectural enhancements over existing Intel mobile processors. The following list provides some of the key features on this processor:

- Supports Intel®Architecture with Dynamic Execution
- High performance, low-power core
- On-die, primary 32-kbyte instruction cache and 32-kbyte write-back data cache
- On-die, up to 2-Mbyte second level cache with Advanced Transfer Cache Architecture
- Advanced Branch Prediction and Data Prefetch Logic
- Streaming SIMD Extensions 2 (SSE2)
- 400/533MHz, Source-Synchronous processor system bus
- Advanced Power Management features including Enhanced Intel SpeedStep® technology
- Micro-FCBGA packaging technologies

Please call Kontron to get the available CPU speed and configuration. See Intel's Web site for additional details about Pentium® M architecture and instruction set.

2.2.2 Chipset Feature

- Processor/Host Bus Support
    - Intel® Pentium® M processor with 1-Mbyte or 2-Mbyte of L2 cache
    - 400/533 MHz system bus (2X address, 4X data)
    - System bus Dynamic Bus Inversion (DBI)
    - 36-bit system bus addressing
    - 12-deep in-order queue
    - AGTL+ bus driver technology with on-die termination resistors
    - Parity protection on system bus data, address/request, and response signals

- Memory System
    - Supports 72 bit, Registered, ECC DDR DIMMs
    - Supports 256 Mb, 512Mb and 1 Gb DRAM densities
    - Cache Latency of 2 and 2.5

- Dual-Channel Support
    - One 144-bit wide DDR memory port (with ECC)
    - Peak memory bandwidth of 3.2 GB/s
    - Supports 2GB of double-sided SODIMMs
    - SODIMMs must be populated in pairs

- Hub Interface_A to ICH3-S
    - 266 MB/s point-to-point Hub Interface 1.5 (8 bit) connection to ICH3-S
    - 66 MHz base clock running 4X data transfers
    - Isochronous support
    - Parallel termination mode only
    - 64-bit addressing on inbound transactions (maximum 16 GB memory decode space)

- Hub Interface_B, Hub Interface_C, and Hub Interface_D
    - 1 GB/s point-to-point Hub Interface 2.0
    - 66 MHz base clock running 8x (1 GB/s) data transfers
    - Supports snooped and non-snooped inbound accesses
    - Parallel termination mode only
    - 64-bit addressing on inbound transactions (maximum 16 GB memory decode space)
    - 32-bit outbound addressing supported for PCI-X

- RASUM
    - Hub Interface_A protected by parity
    - Hub Interface_B–D protected by ECC
    - Memory auto-initialization by hardware implemented to allow main memory to be initialized with valid ECC
    - Memory scrubbing supported

Note:
Many errors can be monitored by setting the DMI event BIOS menu such as ECC errors, parity errors on all PCI/PCI-X buses, and more. See the BIOS section for details.

2.2.3 Memory Interface

This product supports up to two Gigabytes on 2 x 200-pin latching SO-DIMM sockets. Supported memory includes PC-1600/PC-2100 DDR, 2.5V registered SDRAM, non-ECC/ECC mode. The MCH memory controller is capable of up to a nibble error correction and multiple nibble error detection via. There are two DDR channels 72-bit 100/133MHz for interleave operation to match the bandwidth of the CPU front side bus. The memory controller is optimized for applications that use huge amounts of memory and have the following high end feature:

2.2.3.1 Memory scrubbing:

This feature allows the E7501 to automatically correct ECC errors and write back the good data into memory without the CPU intervening. This is done in hardware.

2.3 ICH3-S

2.3.1 Enhanced IDE Interfaces

EIDE interface is part of the ICH3-S south bridge. The interface conforms to the ATA specification and support ATA100 for 100MB/s burst transfer.
The board features two channel Bus Master PCI EIDE dedicated to Primary and Secondary IDE logical interfaces (Secondary Channel is available only through the Rear Transition Module). Each channel supports up to two IDE devices (including CD-ROMs, hard disks and CompactFlash) with independent timings, in Master/Slave combination.

Signal Paths:
The primary IDE Interface is available through the compact flash or through the Mezzanine connector.
The secondary IDE interface is only available through the CPCI I/O connector.

Bios Settings:
- Main
- Specify disk type
- Advanced → PCI Configuration → IDE – Device 31, Function 1
- Enabled or disabled the IDE controller

The IDE interfaces supports PIO mode 4 transfers up to 16.6MB/sec and Bus Master IDE transfer up to 100MB/sec (Ultra-DMA/100).

Note:
Devices connected to IDE0 must be set in cable select so the onboard jumper will set the master and the slave devices.

CAUTION

When connecting IDE devices to the Primary IDE interface, Master and Slave devices must be shared in respect of the device allocation on both the compact flash connector and the mezzanine. Two Master devices must not be installed on the same interface at the same time.
If a device is alone on an interface it shall be master

2.3.2 USB 1.1 Interfaces

USB strengths include:

- Capability to daisy chain as many as 127 devices per interface
- Fast bi-directional
- Isochronous/asynchronous interface
- 12MBPS transfer rate
- Standardization of peripheral interfaces into a single format

USB supports Plug and Play and hot-swapping operations (OS level). These features allow USB devices to be automatically attached, configured and detached, without reboot or running setup.

Pin	Signal
1	VCC
2	DATA-
3	DATA+
4	GND

Signal Paths:
USB0 signals are available on the faceplate from the J11 connector.
Both USB 1 and USB 2 signals are available through the CPCI I/O connector (J3).

Bios Settings:
Advanced → PCI Configuration → Legacy USB Support (keyboard and mouse)

The CP6011 board supports the standard open host controller interface (OHCI) and uses standard software drivers that are OHCI compatible.

2.4 Super I/O

2.4.1 Floppy Disk Interface

The onboard floppy disk controller is IBM PC XT/AT compatible. It handles 3.5", low and high density disks.

Signal Paths:
The floppy disk controller interface is available through the J5 connector.

Bios Settings:
Main → Legacy Diskette A.

Advanced → On-board Device Configuration → Floppy Disk Controller.

2.4.2 PS/2 Keyboard / PS/2 Mouse Interface

The onboard keyboard controller is compatible with 8042 software.

Signal Paths:

PS/2 keyboard and PS/2 mouse signals are available through the J3 CPCI I/O connector.
Keyboard: J3, Row E, pin 2, 3. (See appendix for complete pinout description of J3.)
Mouse: J3, Row E, pin 4, 5

Bios Settings:
Advanced → Boot Settings Configuration → PS/2 Mouse.

2.4.3 Serial Ports

Two fully functional serial ports are provided on the board for asynchronous serial communications. They are 16C550 high-speed UART compatible and support 16-byte FIFO buffers for transfer rates from 50bps to 115Kbps.
Each serial port is specified as follows:

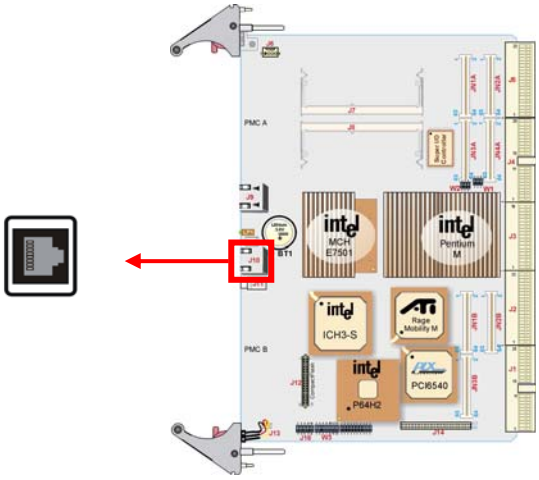
Designation	Communication Mode	Output Path
Serial Port A (COM1)	RS-232	Front Plate RJ-45 (J10), CPCI J3
Serial Port B (COM2)	RS-232/RS422/RS485	CPCI J3

UART registers are individually addressable and fully programmable.

2.4.3.1 Serial Port 1 (J10)

Serial Port 1 is buffered directly for RS-232 operation. Signals include the complete signal set for handshaking, modem control, interrupt generation, and data transfer. When assigned as Serial Port 1, the port is 100% compatible with the IBM-AT serial port in RS-232 mode.

Pin	Signal
1	RTS
2	DTR
3	TXD
4	DCD
5	GND
6	RXD
7	DSR
8	CTS



Note:
The pinout is a custom one, not the same as RS-232D EIA/TIA 561. Use the Kontron provided RJ45 to DB9 adapter.

Signal Paths:
The Serial Port 1 signal is always available in front and rear access.

Bios Settings:
Advanced → On-board Device Configuration → Serial port A.

2.4.3.2 Serial Port 2

Serial Port B is buffered directly for RS-232 operations and is 16C550 PC-compatible. The interface includes the complete signal set for handshaking, modem control, interrupt generation, and data transfer. This port is 100% compatible with the IBM-AT serial port.

Signal Paths:
Serial Port B signals are only available through the J3 CPCI I/O connector.

Related Jumpers:
W4 and W5: insert both jumper if Serial Port 2 is used in RS-422 or RS-485 mode and need termination resistors. Termination resistors are 120-ohm.

Bios Settings:
Advanced → On-board Device Configuration → Serial port B.

Upon a power-up or reset, the Serial Port 2 interface circuits is automatically configured for the operation mode setup in the BIOS. This Serial Port signal assignation on the J3 CPCI I/O connector depends on the operation mode (RS-232, RS-422, or RS-485) it has been set:

J3 Connector		RS-232	RS-422	RS-485
Pin#	Name			
D3	DCD	DCD	RSV	RSV
B3	RX	RXD	RX(-)	RX/TX(-)
C3	DSR	DSR	RSV	RSV
D4	TX	TXD	TX(-)	RSV
A3	RTS	RTS	RX(+)	RX/TX(+)
C4	CTS	CTS	TX(+)	RSV
A4	RI	RI	RSV	RSV
B4	DTR	DTR	RSV	RSV

2.4.3.2.1 RS-232 Protocol

When configured for RS-232 operation mode, the serial port is 100% compatible with the IBM-AT serial port signals.

2.4.3.2.2 RS-422 Protocol

The RS-422 protocol (Full Duplex) uses both RX and TX lines during a communication session.

CAUTION

In RS-422 mode, install W4 and W5 jumper caps to connect the 120-Ohm termination resistors. (See the Jumper Settings section.)

2.4.3.2.3 RS-485 Protocol

The RS-485 protocol (Half Duplex) also uses differential signals during a communication session. It differs from the RS-422 mode because it offers the ability to transmit and receive over the same pair of wires and allows a shared communication line by multiple stations. This configuration (also known as Party Line) allows only one system to take control of the communication line at a time. In RS-485 mode, the RX lines are used as the transceiver lines, and the RTS signal controls the direction of the RS-485 buffer.

When set for RS-485 mode in the BIOS, upon power-up or reset, the transceiver is by default in receiver mode to prevent unwanted perturbation on the line. Party line operation mode requires termination resistors to be installed at both ends of the network.

CAUTION

When installing the board at one end of the network, connect the W4 and W5 jumper caps at the 120 ohms termination resistors (See *Setting Jumpers*).

2.4.4 Ethernet Interfaces

The 2 Ethernet (Intel 82544GC) controllers reside on the PCI-X bus B and run at 133MHz (without PMC B) and is 64-bit wide. Each interface supports 10Base-T/100Base-TX/1000Base-T with auto-negotiation and automatic crossover cable detection, in rear access. The Ethernet (Intel 82551er) controller resides on the PCI bus D and runs at 33MHz at 32-bit wide, this interface support 10Base-T/100Base-TX with auto-negotiation in front access.

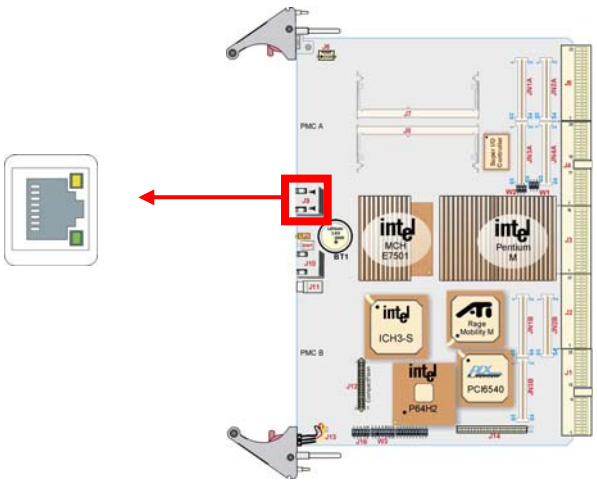
The i82544GC features high performance with TCP/IP and UDP/IP checksum offloading for IPv4 and IPv6, packet filtering, and jumbo frame up to 16K.

The CP6011 has boot from LAN capability (PXE) on the 3 ports. Enable the option from the BIOS Set-up Program. Please refer to Section 5.1, PHOENIX BIOS Set-up Program.

See Kontron's Web site: http://www.kontron.com for the latest drivers.

See Intel's Web site: http://www.intel.com for the latest drivers for the i82544GC and for additional information on the Ethernet controller.

Pin	Signal 10/100
1	TX+
2	TX-
3	RX+
4	N.C.
5	N.C.
6	RX-
7	N.C.
8	N.C.



Signal Paths:
The Ethernet Management RJ45 connector is on the faceplate and the two other LAN connectors are available on rear access.

BIOS Settings:
Advanced → PCI Configuration → On-board Ethernet Controller.

2.4.4.1 CPCI I/O Configuration

In rear access or 2.16 configuration, the two Gig-Ethernet ports are available from a RTM or in a PICMG2.16 system.

CAUTION

1. When using a PICMG 2.16 system, LAN cannot be used on the RTM.
2. You cannot use a standard RTM with most PICMG2.16 systems. See your system's manual.

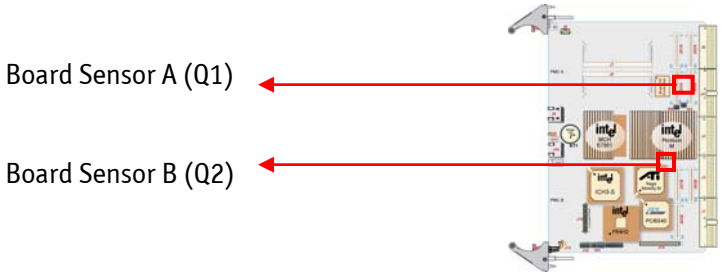
Signal Paths:
10/100 Ethernet is available on J9 in the faceplate.
10/100/1000 2 Ethernet are available through CPCI J3

Bios Settings:
Advanced → PCI Configuration → On-board Ethernet Controller.

2.5 System Management Features

2.5.1 Thermal Management

The SBC includes a user-defined temperature sensor / alarm function, which provides thermal monitoring of the processor, using the WINBOND W83627HF. In addition, the Pentium-M includes an active thermal control circuit (TCC) that can automatically throttle the CPU clock when exceeding the maximum operating temperature.
The current CPU temperature can be read by software or by a user application. Use the IPMI for increased system management. If you would like more information, please consult the IPMI section.



Bios Settings:
Monitoring → Intelligent System Monitoring.

Note:
Temperature values are provided for reference only; they should not be used for system calibration.

CPU overheating may happen if the system fans fail. In the advent of catastrophic overheating, the SBC will power down itself.

Note:
If the CPU overheats, the CPU asserts the THERMTRIP# signal, which stops power. You need to cycle BDSEL# (or remove and insert the board) to restart the board.

2.5.2 Power Supply Monitoring

All onboard supplies are monitored; any low power rail holds the board in reset. Most power rails also can be monitored through the LPC bus by using the WINBOND W83627HF or by using the embedded IPMI controller.

Bios Settings:
Section 5.1.2.6.1.2, Monitoring *Menu Selection, Intelligent System Monitoring, Hardware Monitor Voltage Inputs.*

2.5.3 Programmable Dual Stage Watchdog

A two-stage digital watchdog timer with software programmable time-out period is available. Following a reset of any source, the watchdog is disabled. Software enables the watchdog.

Bios Settings:

- Monitoring → Watchdog After POST (Enable watchdog automatically before OS launch)
- Monitoring → Watchdog Duration
- Monitoring → FPGA IRQ

Software Usage:

- See registers 0x190, 0x191 and 0x196 description in Appendix C for details.
- See Application Note AN030001A for watchdog timer usage (This App note gives bad info on CP6011 0x192, 0x196, 0x190 register.)

2.6 Video Interface

The video controller, ATI Mobility-M, with its integrated 4MBcapable of CRT resolutions up to 1600 x 1200 x 65K colors (4MB RAM).
The video interface features high performance 32-bit frame buffer PCI video.

Signal Paths:
Video signals are available through J3 CPCI connector.

Related Jumpers:
W2(5-6) enables or disables the onboard video.
See Section 3.1 – *Jumper Settings*.

Bios Settings:
Advanced → PCI Configuration → Default Primary Video Adapter.

- CPCI I/O Configuration
  VGA interface signals are available on the J3 CPCI I/O connector.

2.6.1 Supported Resolutions

The maximum video resolution and performance depend directly on the drivers running with your software application. Resolution and number of colours specification are listed below:

Resolution	Number of Colours
640x480, 800x600, 1024x768, 1280x1024, 1600x1200	256 (8 bits)
640x480, 800x600, 1024x768, 1280x1024, 1600x1200	65,536 (16 bits)
640x480, 800x600, 1024x768, 1280x1024	16.8 million (24 bits)
640x480, 800x600, 1024x768	16.8 million (32 bits)

2.6.2 Major Features Description

- VGA Compatibility
  The video controller includes all registers and data paths required for the VGA controller and supports extensions to VGA, including resolutions up to 1600 x 1200 x 65K colours non-interlaced. The 24-bit images are displayed at up to 1280x1024 resolutions.

- 2D Graphics Engine
  The 2D graphics engine is an advanced 32-bit, three-operand engine that accelerates BitBLTs as line draws, polygon draw, and polygon fill. The 2D graphics engine also performs video and bitmap scaling, and data overlay.

2.7 CPCI Features

2.7.1 Universal Bridge (PLX6540)

This cPCI product's access to the backplane bus runs through the PLX6540 PCI-X to PCI-X universal bridge. The feature set of this bridge is similar to the HB6, which is used on Kontron cPCI products. The PLX6540 can operate in either 32 or 64 bits bus width and with any PCI or PCI-X frequency up to 133MHz.

2.7.1.1 Transparent Mode

When the CP6011 is inserted in the system slot of a backplane, the bridge is configured in transparent mode and performs like any other bridge. You can configure important registers from the BIOS setup. The board will power up depending on board options (system slot 3.3V or 5V).

2.7.1.2 Nontransparent Mode

If the SBC is inserted in a peripheral slot, the PLX6540 will be configured in nontransparent mode and will be seen as an I/O device. By default, it will appear with vendor ID 3388h and device ID 0029h. The PLX6540 will always claim a 16MB window unless the default is changed in the EEPROM settings. The board will work in either a 3.3V or 5V backplane.

2.7.1.3 *Busless Operation*

When used in a busless slot, as in some PICMG2.16 systems, the bridge will be disabled and will disappear from the PCI device list.

2.7.1.4 *Using the EEPROM*

If you use this product as an I/O board, you can assign different vendor ID and device ID to the PLX6540 and can configure the PCI resources that will be claimed at boot up. This allows the CP6011 to act as an I/O board, like any other peripheral device (SCSI, Ethernet) and to load proper drivers. Please contact Kontron's technical support if you need to configure the EEPROM.

Related Jumpers:
W6-W7-W8 allow you to set maximum bus speed or disable the bridge.

Bios Settings:
Advanced → PCI Configuration → PCI Performance settings → PLX6540 (HB8) related options.

2.7.2 Hot Swap

2.7.2.1 *Power Ramping and Overcurrent Protection*

This product has electrical components that control current ramp-up on the board when the board is hot swapped in the chassis. Current transient upon insertion follows the PICMG2.1R2.0 specification.
The hot swap circuit also protects from overcurrent. If for any reason current requirements increase to an abnormal level, the board will shut down. Power cycling or board select (BDSEL# signal) cycling restarts the board.

2.7.2.2 *Hardware Connection Process*

If you would like more information, please see Section 1.5.4 for technical background. This section explains how to use the ENUM# signal.
When the board is used in a system slot, it is possible to detect insertion and pending extraction of a compliant peripheral cPCI card.

WARNING

1. Some mechanical parts of the guide-rail are fragile (shield contacts and clips). Do not use force to insert and connect a CompactPCI module.
2. If there is any mechanical resistance while you insert a module, ensure there is no mechanical obstacle and verify that all parts are well aligned.

2.7.3 Bus Mode

The PICMG2.0R3.0 specification and PICMG2.1R2.0 specification do not dictate how to support a PCI-X card. This product implements a solution that is the best candidate for the next revision of this specification.
Bus-speed negotiation is always done on a PCI reset. Inserting a board in a live system will never make the bus not function with compliant hardware. A peripheral card will have a problem if the bus is faster than the card's capability. In other cases, the card should initialize itself with the current bus mode.

2.8 IPMI

This product fully supports Intelligent Platform Management Interface 1.5 (IPMIv1.5) and PICMG2.9R1.0 specifications. All its functionalities run under an autonomous management controller even if the board is held in reset or power down by a management card within a system design for High Availability such as XL-VHDS and XL-LP42.

While the CP6011 IPMI implementation is fully compliant to IPMI v1.5 and should work with any System Management Software that respect this specification, it has been design to be easily integrate with the Service Availability Forum-Hardware Platform Interface (SAF-HPI) specification.

You can find more information about the SAF-HPI at the following Web site:

http://www.saforum.org/home

2.8.1 Technical Background

IPMI is an extensible and open standard that defines autonomous system monitoring. It is autonomous because all management controllers within a compact PCI chassis monitor its own sensors and send critical events through a dedicated bus to a Baseboard Management Controller (BMC) that logs it into a non volatile System Event Log (SEL). The CP6011 IPMI implementation include a device SDR module that allows the user's System Management Software (SMS) to discover all system's components and to build a database of all management controller sensors.

You can find more information about the IPMI at the following Web site:

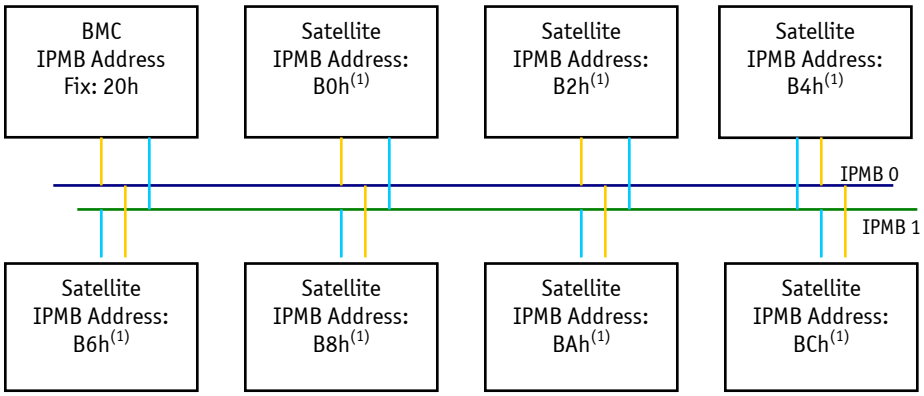
http://www.intel.com/design/servers/ipmi/index.html

2.8.1.1 *IPMI Glossary*

IPMI	Intelligent Platform Management Interface
BMC	Baseboard Management Controller In a compact PCI chassis, there can be only one BMC present. The BMC includes de SEL and the SDRR for the complete system. The BMC is connected to the other blades in the system via a dedicated bus (IPMB). The CP6011 management controller can be set in BMC by selecting the option in the BIOS setup menu.
SMC	Satellite Management Controller In a compact PCI chassis, there can be many SMC. Each SMC is connected to the BMC via a dedicated bus (IPMB). The CP6011 management controller can be set in SMC mode by selecting the option in the BIOS setup menu.
SEL	System Event Log The SEL is present only in the BMC. If an event occurs in any blade, the sensor event is sent throught the IPMB bus (if SEL is not local) and stored in the BMC SEL.
SDR	Sensor Data Record This is the IPMI data structure that defines a sensor.
SDRR	Sensor Data Record Repository The SDRR is only present witin the BMC. Usually, the SDRR contains all management controller SDRs of the chassis. A Kontron utility named 'fillsf.exe' is provided in the IPMI DOS tool package to make a full chassis discovery and fill the SDRR with the found SDRs. The factory default repository contains only the local board SDRs.
IPMB	Intelligent Platform Management Bus The dedicated I2C management bus where SMC communicate with the BMC.
KCS	Keyboard Controller Style This is the IPMI mandatory interface on the host system to communicate with the BMC.
FRU Data	Field Replaceable Units inventory Data A FRU inventory data is available in all management controller. The FRU contains information about the product such as the part number and the serial number. See PICMG Specification 2.9 for complete details on the FRU inventory data byte structure. . A Kontron utility named Fillsf.exe is provided to update the FRU inventory data.
SMS	System Management Software This is the generic term for the high level software that perform all management task.
SAF-HPI	The SAF Hardware Platform Interface (HPI) provides an industry standard interface to monitor and control highly available telecommunications system platforms. The ability to monitor and control these platforms is provided through a consistent and standard set of programmatic interfaces. HPI provides the interface between the SMS and IPMI, allowing portability of SMS across many different hardware platforms and portability of hardware platforms across many different SMS.
PMM	The Platform Management Module is in charge of performing all management actions from chassis point of view. From hardware perspective it is the BMC within the system that collect all events coming from any SMC. It is also in charge to perform the slot power/reset control action. From management point of view, the PMM includes the SAF-HPI layer that gives to SMS access to all chassis sensor/control. The PMM is part of Kontron XL-VHDS chassis.

2.8.1.2 *IPMI in a Compact PCI Chassis*

Kontron IPMI implementation in cPCI environment is compliant to the PICMG2.9R1.0 specification. The specification gives the pinout of J1 and J2 as well as the addressing scheme. There should be only one BMC in the chassis. The BMC may reside either on an SBC blade or on an external Platform Management Module (PMM), the specification gives full latitude over this.



(1) IPMB address for satellite is determined via the location of the slot in the chassis.

2.8.1.3 *IPMI Setup*

To use the IPMI resources in a system, some steps are needed. The system operator must perform Step 1. The SMS application performs Steps 2 and 3.

1. Elect a BMC by setting the management mode to BMC in the BIOS Setup Menu. By default, all Kontron's CPCI blades are configured in SMC mode.
2. Fill the SDRR with all the present sensors in the chassis. This step may be done using the *fillsf.exe* Kontron utility in DOS. IPMI specification requires the SDRR to be rebuild each time there is a configuration change in the chassis. For more details about Fillsf.exe please refer to CP6011_IPMI_Firmware package on Kontron website.
3. Probe the BMC SEL for event or any other available information using the SMS of your choice or by sending the command directly using your own tool.

2.8.2 IPMI Implementation of CP6011

2.8.2.1 *Key Features*

- Compliant with IPMI specification 1.5, revision 1.1
- Compliant with PICMG 2.9 specification
- Can be configured as BMC or SMC by software from the BIOS Setup Menu
- Firmware designed and specially made for compact PCI implementation and easy integration with SAF-HPI such as the Kontron XL-VHDS SAF-HPI implementation.
- KCS SMS interface with interrupt support

- Dual Port IPMB configurable as two independent channels or in redundant mode via BIOS Setup Menu
- Out of band management and monitoring using IPMB interface permits access to sensors regardless of SBC state
- Sensor threshold fully configurable
- Sensor name prefixed with slot number
- Complete IPMI watchdog functionality
- Complete SEL, SDR repository and FRU inventory data functionality
- Master Read/Write I2C supports for external I2C devices communications (additional FRU inventory data, EEPROM, FAN)
- Firmware can be updated in the field
- Firmware fully customizable per customer needs
- Interoperable with other IPMI solution

2.8.2.2 IPMI commands set on CP6011

The next table presents the supported IPMI commands within the CP6011. All these commands are compatible to IPMI v1.5 and PICMG 2.9 specification.

Global commands
Get Device ID
Cold Reset
Get Self Test Results
Broadcast 'Get Device ID'

BMC-System Interface
Set BMC Global Enables
Get BMC Global Enables
Clear Message Flags
Get Message Flags
Enable Message Channel Receive
Get Message
Send Message
Read Event Message Buffer
Get BT Interface Capabilities
Master Write-Read I2C

BMC Watchdog Timer
Reset Watchdog Timer
Set Watchdog Timer
Get Watchdog Timer

FRU Inventory Device
Get FRU Inventory Area Info
Read FRU Inventory Data
Write FRU Inventory Data

SEL Device Commands
Get SEL Info
Get SEL Allocation Info
Get SEL Info
Get SEL Allocation Info
Reserve SEL
Get SEL Entry
Add SEL Entry
Delete SEL Entry
Clear SEL
Get SEL Time
Set SEL Time

SDR Repository Device
Get SDR Repository Info
Get SDR Repository Allocation Info
Reserve SDR Repository
Get SDR
Partial Add SDR
Delete SDR
Clear SDR Repository
Run Initialization Agent

Event Commands
Set Event Receiver
Get Event Receiver
Platform Event

Sensor Device
Get Device SDR Info
Get Device SDR
Reserve Device SDR Repository
Set Sensor Hysteresis
Get Sensor Hysteresis
Set Sensor Threshold
Get Sensor Threshold
Set Sensor Event Enable
Get Sensor Event Enable
Get Sensor Reading

PICMG IPMI extension
Set FRU LED State
Get FRU LED State
Get FRU LED Properties
Get LED Color Capabilities

OEM Command
Get Init Agent Last Error

2.8.2.3 *Sensors Implemented on CP6011*

The IPMI CP6011 management controller includes many sensors such as voltage or current monitoring and others for pass/fail type signal monitoring. Each sensor's definition is available from the IPMI Device SDR module witch is accessible to the SMS. The following sensor are implemented on the CP6011, the sensor name prefix SXX are dynamically assigned at power up base on cPCI slot number.

Sensors Names	Sensor Type/ Reading Class	Description
SXX:Watchdog	Watchdog 2/ Watchdog 2 specific	IPMI watchdog
SXX:IPMB0 Stuck	Cable-interconnect/ digital-discrete	PICMG 2.9 required sensor, indicates problem on IPMB0.
SXX:IPMB1 Stuck	Cable-interconnect/ digital-discrete	PICMG 2.9 required sensor, indicates problem on IPMB1.
SXX:IPMI info-1	OEM/OEM specific	Reserved for internal firmware usage.
SXX:IPMI info-2	OEM/OEM specific	Reserved for internal firmware usage.
SXX:InitAgent Err	OEM/digital-discrete	Only present on BMC. Indicates if the Init. Agent has enconter a problem (such as missing SMC).
SXX:Power Off	Power Supply / OEM specific	Indicates any source holding board in power down.
SXX:Board Reset	OEM/OEM specific	Indicates any source holding board in reset.
SXX:Power Good	Power Supply/ OEM specific	Reflect goodness of various on board supply
SXX:Temp-A (Q1)	Temperature/ threshold	Upper Edge (PMC site A) board temperature.
SXX:Temp-B (Q2)	Temperature/ threshold	Lower Edge (PMC site B) board temperature.
SXX:CPU Temp	Temperature/ threshold	Current CPU temperature on-die thermal diode.
SXX:Board 12V	Voltage/ threshold	Board 12V supply.
SXX:Board –12V	Voltage/ threshold	Board –12V supply.
SXX:Volt Battery	Voltage/ threshold	Board RTC battery.
SXX:Slot System	Entity presence/ Ent. pres. specific	Indicated if board is in a system slot.
SXX:PSU status	Power Supply/ P. Supply specific	System power supply Deg/Fail indication.
SXX:Lan1 Link	LAN/LAN Specific	LAN1 link status (PCI bus X, device 0 function 3)
SXX:Lan2 Link	LAN/LAN Specific	LAN2 link status (PCI bus X, device 0 function 2)
SXX:Lan3 Link	LAN/LAN Specific	LAN3 link status (PCI bus X, device 1 function 0)
SXX:Board 1.2V	Voltage/threshold	Board 1.2V supply
SXX:Board 2.5V	Voltage/threshold	On board DC-DC converter from 3.3V. Mainly used for memory.
SXX:Board 1.8V	Voltage/threshold	Board 1.8V supply
SXX:IPMI/IPMB 5V	Voltage/threshold	Voltage provided for external IPMB bus.
SXX:Board 5V	Voltage/threshold	Board 5 Volts supply
SXX:Board 3.3V	Voltage/threshold	Board 3.3 Volts supply
SXX:Board Icc 5V	current/threshold	Total current from baseboard and mezzanine on 5V supply.
SXX:Board Icc 3V	current/threshold	Total current from baseboard and mezzanine on 3.3V supply.
SXX:Board NMI	Critical interrupt/ digital-discrete	CPU NMI interrupt has occur.
SXX:SMI Timeout	Critical interrupt/ digital-discrete	CPU remain in SMI interrupt state for to much time.
SXX:PMC-A	Entity presence/ Ent. pres. Specific	Indicated if upper mezzanine (PMC Site A) is installed.
SXX:PMC-B	Entity presence/ Ent. pres. specific	Indicated if bottom mezzanine (PMC Site B) is installed.
SXX:Slot State	Slot-Connector/ Slot-Con. specific	Information about: board ejector,power off, fault status.
SXX:CPU status	Processor/ processor-specific	CPU Thermal trip alarm.
SXX:CPU Throttle	Processor/ digital-discrete	Thermal over heat indication, CPU throttling in action.
SXX:IPMB1 Alert	Cable-interconnect/ digital-discrete	PICMG 2.9 required sensor, device on IPMB1 require attention.
SXX:PCI Present	Entity presence/ Ent. pres. specific	Indicates if the backplane is PCI enabled(otherwise, PICMG 2.16 might be present)
SXX:PCI VIO Error	Power Supply/ digital-discrete	System slot in VIO 5V CPCI backplane
SXX:PMC VIO Error	Power Supply/ digital-discrete	PMC VIO Error, check VIO jumpers.
SXX:Slink Error	Management Subsystem Health/ specific	Indicates if the management Slink is recognized

2.8.3 High Availability Facilities

2.8.3.1 IPMI extension for control

You will find below the standard IPMI formatted commands that may be used within a High Available System that use abstraction layer such as SAF-HPI.

- Set FRU LED State

The "Set FRU LED State" command allows the state of the FRU LEDs to be controlled by the SMS. On the CP6011, the command provides facilities to control the BLUE hot-swap indicator LED.

	Byte		
Response command	1	NetFn Group Extension request/LUN:	B0
	2	Command ID:	07
	3	cPCI ID Extension	00
	4	FRU Device ID	00
	5	LED ID 00h = BLUE Hot-swap LED	00
	6	*LED Function* 00h = LED OFF Override 01h - FAh = LED BLINKING Override. The off duration is specified by the value of this byte and the on duration is specified by the value of byte 7. Both values specify the time in tens of milliseconds (10ms -2.5s) FBh = LAMP TEST state. Turn on LED for duration specified in byte 7 (in hundreds of milliseconds) then return to the highest priority state. FCh = LED state restored to Local Control state FDh-FEh Reserved FFh = LED ON Override	XX
	7	*On-duration*. LED on-time in tens of milliseconds if (1 ≤ Byte 6 ≤ FAh) Lamp Test time in hundreds of milliseconds if (Byte 6 = FBh. Lamp Test time value must be less than 128. Other values when Byte 6= FBh are reserved. Otherwise, this field is ignored and **shall** be set to 0h.	XX
	8	*Color when illuminated* 01h = Use BLUE 0Eh = Do not change 0Fh = Default color	XX
Response command	1	NetFn Group Extension response/LUN:	B4
	2	Command ID:	08
	3	Completion code:	00
	4	cPCI ID Extension	00

- Get FRU LED State

The "Get FRU LED State" command returns the state of the FRU's BLUE hot-swap LED, including whether a Lamp Test or Override state is enabled for it.

	Byte		
Request command	1	NetFn Group Extension request/LUN:	B0
	2	Command ID:	08
	3	cPCI ID Extension	00
	4	FRU Device ID	00
	5	LED ID 00h = BLUE Hot-swap LED	00
Response command	1	NetFn Group Extension response/LUN:	B4
	2	Command ID:	08
	3	Completion code:	00
	4	cPCI ID Extension	00
	5	*LED State* [7-3] = reserved [2]–1b if Lamp Test has been enabled [1]–1b if Override has been enabled [0]–1b if Local Control has been enabled	XX
	6	*Local Control LED Function* 00h = LED is OFF. FFh = LED is ON	XX
	7	*Local Control On-duration*. Local control Blinking state is not supported; this byte will be set to 0h.	00
	8	*Local Control Color* 01h = BLUE	01
	[9]	*Override state LED Function*. This byte is returned if either Override state or Lamp Test is in effect. 00h = LED Override state is OFF. 01h - FAh = LED Override state is BLINKING. The off duration is specified by the value of this byte and the on duration is specified by the value of byte 10. Both values specify the time in tens of milliseconds (10ms -2.5s). FBh - FEh = Reserved FFh = LED Override state is ON	XX
	[10]	*Override state On-duration*. This byte is returned if either Override state or Lamp Test is in effect. The LED on-time in tens of milliseconds if (01h ≤ Byte 7 ≤ FAh) and 0h otherwise.	XX
	[11]	*Override State Color* 01h = BLUE	01
	[12]	*Lamp Test Duration*. This byte is not returned if Lamp Test is not in effect. This byte contains the Lamp Test remaining time in hundreds of milliseconds.	XX

- Get FRU LED Properties

The "Get FRU LED Properties" command allows SMS to determine which of the LEDs, if any, are under control of the IPM Controller. The CP6011 only support control of BLUE hot-swap LED.

	Byte		
Response command	1	NetFn Group Extension request/LUN:	B0
	2	Command ID:	05
	3	cPCI ID Extension	00
	4	FRU Device ID	00
Response command	1	NetFn Group Extension response/LUN:	B4
	2	Command ID:	05
	3	Completion code:	00
	4	cPCI ID Extension	00
	5	*General Status LED Properties* A bit field indicating the FRU's ability to control the LEDs [7-4] reserved set to 0 [3-1] unused set to 0 [0] - 1b = BLUE LED	01
	6	*Application Specific LED Count* None for CP6011	00

- Get LED Color Capabilities

The "Get LED Color Capabilities" command allows SMS interrogation of the colors supported by each LED. This command is used to determine the valid set of colors prior to issuing a "Set FRU LED State" command. The CP6011 only support BLUE color for BLUE hot-swap LED.

	Byte		
Request command	1	NetFn Group Extension request/LUN:	B0
	2	Command ID:	06
	3	cPCI ID Extension	00
	4	FRU Device ID	00
	5	LED ID 00h = BLUE Hot-swap LED	00
Response command	1	NetFn Group Extension response/LUN:	B4
	2	Command ID:	06
	3	Completion code:	00
	4	cPCI ID Extension	00
	5	*LED Color Capabilities* A bit field. When the bit set, the LED supports the color. Bit LED [7] Reserved, **shall** be set to 0. [6-2] unused for CP6011 [1] LED supports BLUE [0] Reserved, **shall** be set to 0.	01
	6	*Default LED Color in Local Control State* Bits number [7:4] Reserved shall be set to 0. [3:0] Hex Value Function - 1h BLUE	01
	7	*Default LED Color in Override State* Bits number [7:4] Reserved shall be set to 0. [3:0] Hex Value Function - 1h BLUE	01

2.8.4 Software Support

2.8.4.1 IPMI KCS Support in Different OS

For customer that plan to design software using IPMI feature, there are some tools publicly available:

Linux

An open source KCS driver is available for Linux. This driver includes all the necessary functionality (and more) to communicate with the IPMI management controller. http://openipmi.sourceforge.net.

IPMItool is a simple command-line interface to systems that support the Intelligent Platform Management Interface (IPMI) v1.5 specification. It provides the ability to read the SDR and print sensor values, display the contents of the SEL, print FRU inventory data information, it is also capable of using a system interface as provided by a kernel device driver such as OpenIPMI.
http://ipmitool.sourceforge.net

Intel provides some Linux KCS reference drivers; they are available at the following address: http://www.intel.com/design/servers/ipmi/ipmi_driver.htm.

Contact Kontron's technical support for additional tools or help with Linux IPMI tools.

Windows

Intel provides some Windows KCS reference drivers; they are available at the following address: http://www.intel.com/design/servers/ipmi/ipmi_driver.htm

For Windows XP, Windows Server 2003, and Windows 2000, Microsoft is providing a device driver and manageability infrastructure for developers to use to write hardware device drivers. This infrastructure allows management data to be obtained from hardware interfaces that might not have direct, native support in these versions of Windows. By using WMI and WDM, hardware interfaces such as IPMI can be supported in systems.
http://www.microsoft.com/whdc/hwdev/driver/WMI/WMI-intro.mspx

2.8.4.2 Firmware Update

The IPMI firmware update tool *ipmifwu* is available from Kontron for both Dos and Linux. This utility allows you to upload a new binary file to the microcontroller. Consult the *ipmifwu* usage display for complete utility options (by running *ipmifwu–h*). Visit the Kontron Web site for package and firmware availability or call Kontron Technical Support.

DOS Firmware update procedure:

1. Boot DOS.
2. Place both firmware binary and utility 'ipmifwu.exe' on a floppy.
3. Insert the floppy and run the following: *ipmifwu –f firmware.bin –p –r*

Linux Firmware update procedure:

1. Put *ipmifwu* and *firmware.bin* in a temporary directory : i.e: ~/tmp
2. Move to that directory : i.e: cd ~/tmp
3. Simply run the command: ./ipmifwu -f firmware.bin -p -r

Note:
You must have super user (root) privileges to gain access to the hardware ports.

WARNING

Some firmware might not be compatible with some BIOS versions. Always upgrade the BIOS and firmware as recommended.

2.8.5 IPMI Communication LED

It is possible from the BIOS Monitoring Menu to reconfigure IDE LED activity as IPMI communication LED. The meaning of the blink pattern is explained within the table below:

IPMI LED

Led Color	RED		GREEN	
Normal status	**OFF**		**SLOW BLINKING**	
Blinking speed	Slow (100 msec ON; 1.4 sec OFF)	Fast 8 x (150 msec ON; 50 msec OFF)	Slow (250 msec ON; 3 sec OFF)	Fast 8 x (150 msec ON; 50 msec OFF)
Signification	Management Controller request attention to SMS (this may occur when there is a message waiting for the SMS).	Send/ Receive data through the IPMB interface	The Management Controller is running normally; it's an heart beat	Send/ Receive data through the KCS interface

Bios Settings:
Monitoring → IDE Activity Led.

2.9 Debugging Features

2.9.1 Bi-color Debug LED (BLUE/USER LED)

The board has a bi-color LED that is very useful to debug. (Consult the quick reference sheet.) The significance of the LED is context dependent and is shown below.

Time	LED usage
Misconnection on PMC VIO jumper	Both red LEDs will light
During reset.	Blue LED is ON
After reset, during the boot process.	Postcode blinker (blinking)
After the boot process, while the operating system loads.	GREEN and RED is not used.
While the application software runs.	GREEN and RED is not used.
	Application software uses the LED to display status information.

Software Usage:
See register 0x19A description in Appendix C for details.

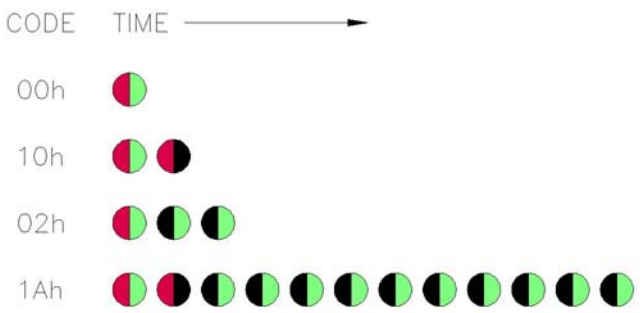
Bios Settings:
Monitoring → IDE Activity Led.

2.9.1.1 POST Code Blinker

The postcode blinker circuit uses a blinking sequence to display the current POST (Power On Selft Test) code value on faceplate. This sequence restarts every time the POST codes value changes. Because POST codes changes all the time during a normal boot process, the blinker does not have enough time to complete its sequence and the debug LED blinks meaninglessly.
If the boot process succeeds, the POST code value has no interest and the BIOS will disable the post code blinker before the operating system launches.
If the boot sequence fails or the CPU hangs, the postcode blinker remains operational and repeats indefinitely the last postcode blink sequence defined below.

1. Blink simultaneously RED and GREEN one time: start of the sequence.
2. Blink RED “R” times while GREEN stays off. “R” range from 0 to 15.
3. Blink GREEN “G” times while RED stays off. “G” range from 0 to 15.
4. Repeat the sequence. (See step 1.)

“R” is the first (most significant) digit of the post code value in hexadecimal; while “G” is the second digit (i.e. post code value is RGh). Some examples are shown in the following figure.



2.9.1.2 Application Software Use of the Debug LED

A status LED can be very useful for software development and for system level troubleshooting. Consult register 0x19A description for software usage (Appendix C).

2.9.2 Serial Post Codes

The 8-bit content of I/O address 80h is serialized into a proprietary protocol and output on J3 connector. In manufacturing, Kontron use a display board to deserialize and display the post code value on 7-segment LEDs modules.
This approach enables you to see post codes because it is not possible to see postcode with a PCI card on CP6011, the PCI to PCI bridges (P64H2 also) does not forward this IO (80h).
The display board is not offered with this product. It is used for manufacturing.
Postcodes can be a useful tool when debugging application software. If the display board is interesting you, please ask your Kontron representative for it.

2.10 Miscellaneous Features

2.10.1 Serial Number

A DS2401 silicon serial number comes standard on the CP6011. It can be read from register 0x193. (See appendix C).

3. Installing the board

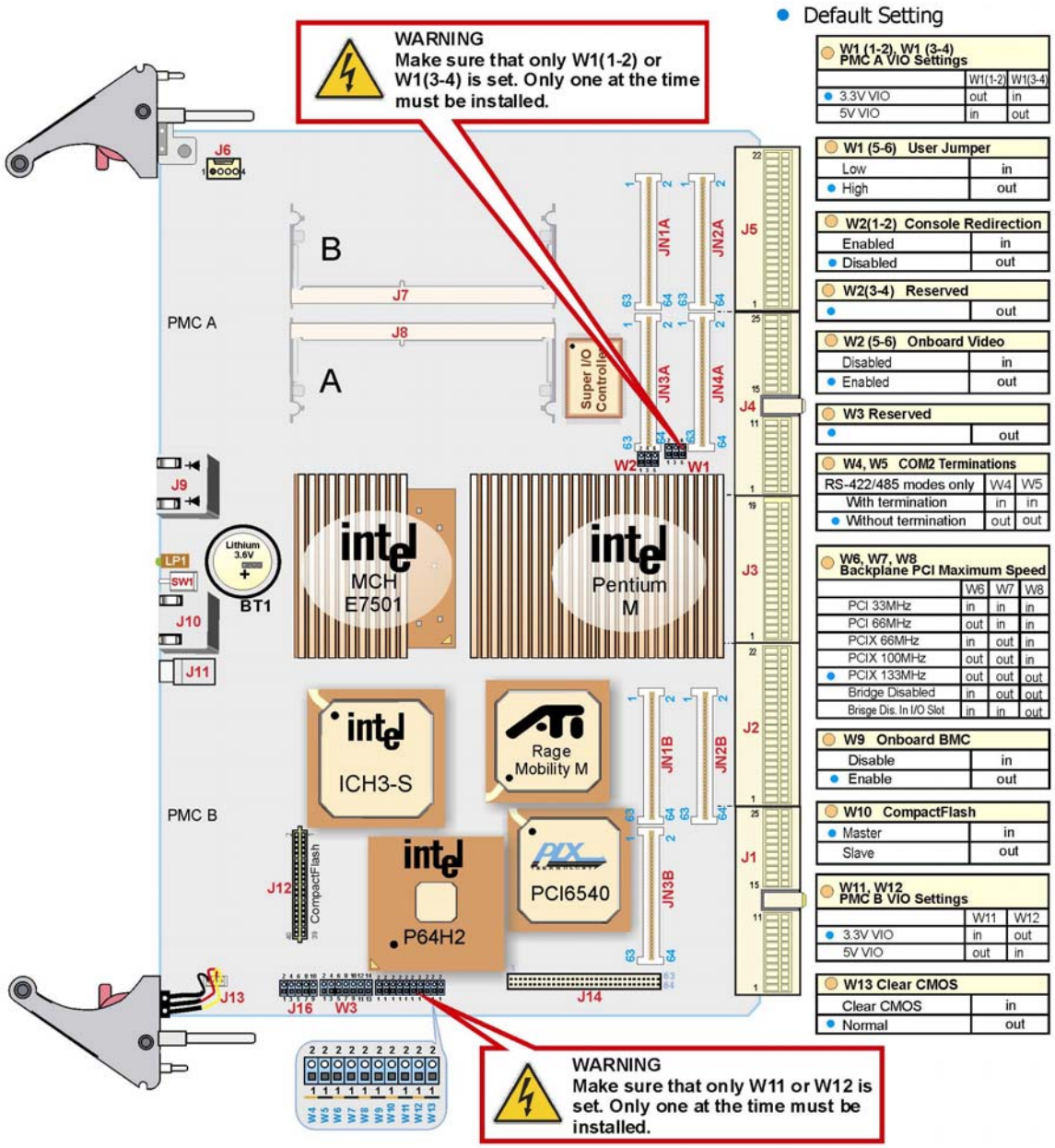
Contents

3.1 Setting Jumpers

3.1.1 Jumper Description

Description		
PMC A VIO Settings	To set the VIO of the PMC A to 3.3V or 5V	**W1(1-2) W1(3-4)**
User Jumper	This jumper is for user applications	**W1 (5-6)**
Console Redirection	To enable the Console Redirection Mode, put the jumper in.	**W2 (1-2)**
Reserved	Reserved	**W2(3-4)**
Onboard Video	Use this jumper to disable the onboard video feature.	**W2 (5-6)**
Reserved	Reserved	**W3**
Serial COM2 Termination	Use these jumpers to connect or disconnect the termination resistors on/from Serial COM2 when set for RS-422/RS-485 operation mode 0.	**W4** **W5**
Backplane PCI	Sets the maximum speed (66/100/133MHz) of the PCI bus located on the backplane	**W6 W7 W8**
Onboard BMC	To disable the BMC, put the jumper in.	**W9**
Compact Flash	To put the CompactFlash in master mode, put the jumper in	**W10**
PMC B VIO Settings	To set the VIO of the PMC B to 3.3V or 5V	**W11 W12**
Clear CMOS	To clear the CMOS, put the jumper in.	**W13**

3.1.2 Setting Jumper & locations



3.2 Processor

This product ships with the CPU installed and a thermal solution. Because the thermal solution is a custom one and the thermal interface is critical for passive cooling, Kontron does not guarantee thermal performance if the heat sink is removed and then reinstalled by the end user.

3.3 Memory

Only use validated memory with this product. Currently recommended configuration and part numbers are:

Quantity of memory	Memory Slot A (J7) (Kontron Part Number)	Memory Slot B (J8) (Kontron Part Number)
512 MB	635-118	635-118
1 GB (1024 MB)	635-119	635-119
2 GB (2048 MB)	635-137-00	635-120

Memory should have the following characteristics:

- DDR200 or DDR266
- 2.5V only
- Single-sided or double-sided
- 1 layer of BGA on PCB side
- X4 or X8 configuration supported
- Serial Presence Detect (SPD) EEPROM
- 64-bit and 72-bit DIMMs supported
- 1.45 inch maximum height

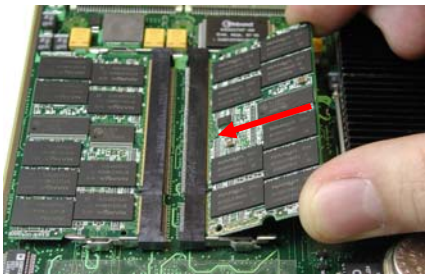
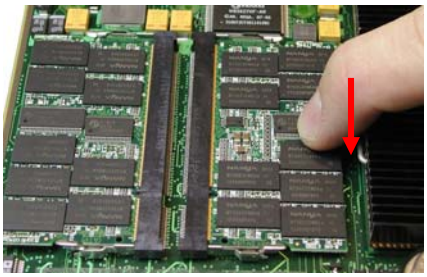
Note:
To ensure proper operation, the board must have two identical memory modules installed. The EEPROM may conflict with the connector's clip. In this case, the two SO-DIMM shall be different. The EEPROM is installed on the 2 different sides. Insert the SO-DIMM with the EEPROM on the upper side.

WARNING

Because static electricity can cause damage to electronic devices, take the following precautions:

- Keep the board in its anti-static package, until you are ready to install memory.
- Wear a grounding wrist strap before removing the board from its package; this will discharge any static electricity that may have built up in your body.
- Handle the board by the faceplate or its edges.

3.3.1 Installing Memory

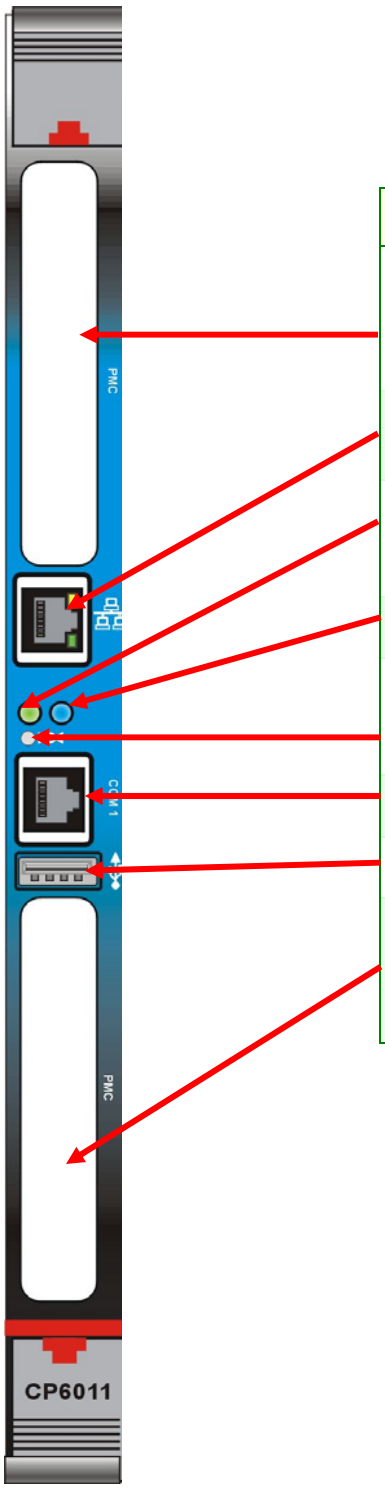
On an anti-static plane, place the board so that you are facing the SO-DIMM sockets	
Insert the SO-DIMM into any available socket, aligning the notches on the module with the socket's key inserts. The EEPROM may conflict with the connector's clip. (1GB only) In this case, the two SO-DIMM shall be different. Insert the SO-DIMM with the EEPROM on the upper side.	
Push down the SO-DIMM until the retaining clips on each side.	
Repeat these steps to populate the other socket.	
To remove a SO-DIMM from a socket, push sideway the retaining clips on each side of the socket, to release the module. Pull out the memory from the socket.	

3.4 Onboard Interconnectivity

3.4.1 Onboard Connectors and Headers

Description	Connector	Comments	
CompactPCI Bus	J1/J2	J1- CPCI bus signals and power. J2- 64 bit extension, arbitration, clocks, reset and power.	
CompactPCI I/O	J3	Serial Ports A and B, LAN 0 and 1, PS/2 Keyboard and Mouse, VGA, and USB.	
CompactPCI I/O	J4 (SCSI)	SCSI (SCSI board version).	
CompactPCI I/O	J4 (PIM)	Mezzanine signals (PIM board version).	
CompactPCI I/O	J5	Legacy connections (IDE and Floppy).	
POST Code	J6	4-pin locking	
Memory Sockets	J7-J8	SO-DIMM 200-pin (Registered DDR-200/266 SDRAM)	
Ethernet Management	J9	RJ-45 connector with built-in activity and link indicators (faceplate)	These connectors are located on faceplate
Serial Port 1	J10	Supports RJ-45 connector (faceplate).	
USB	J11	4-pin USB connector (faceplate).	
Reset	SW1	Reset Switch (faceplate)	
Compact Flash	J12	Compact Flash connector for a T069 Mezzanine	
Hot Swap	J13	Hot Swap Switch	
IDE	J14	IDE mezzanine connector	
JTAG	J16	JTAG connector	
Battery	BT1	CMOS backup battery connector	
PCI Mezzanine	JN1A-JN4A	64-Bit PCIX Mezzanine & PIM	
PCI Mezzanine	JN1B-JN4B	64-Bit PCIX Mezzanine	

3.4.2 Front Plate Connectors and Indicators

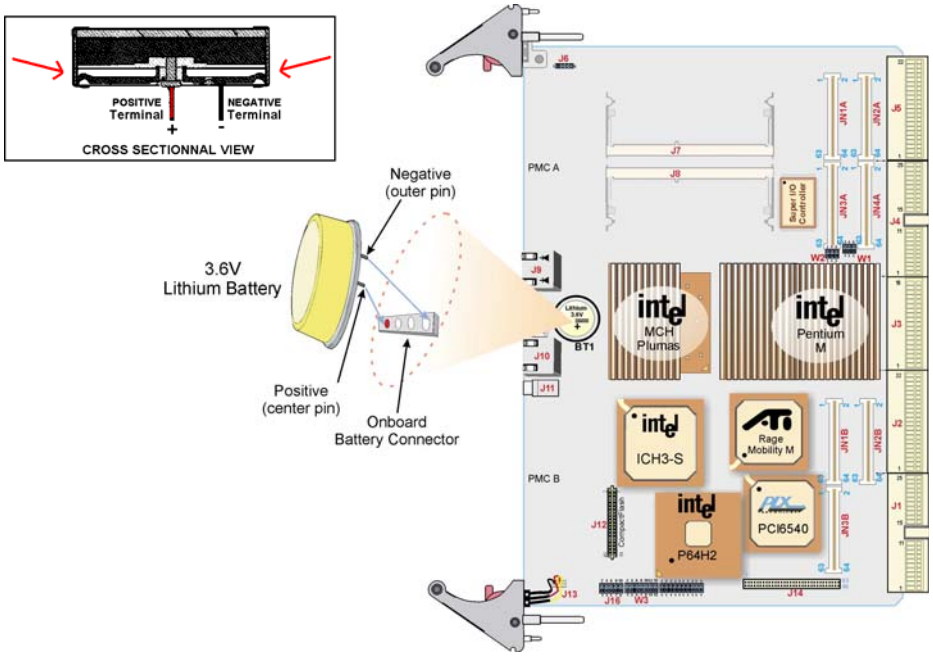


Name	Description	Comments
PMC A	Mezzanine	The front plate supports a PMC cutout and a cap that also acts as an EMI shield when there is no PMC device installed.
J9	Ethernet Management	Ethernet RJ-45 connectors with built-in activity and link indicators
Blue / User LED	Ready to Swap	Lights when the board is ready to be swapped. Display POST code during boot process.
User LED	HDD Activity	Indicates activity on IDE
SW1	Reset Button	Use a small tool to press the button and proceed to a hardware reset of the board
J10	Serial Port A	Standard 8-pin RJ-45 connector
J11	USB0	4-Pin standard USB connector
PMC B	Mezzanine	The front plate supports a PMC cutout and a cap that also acts as an EMI shield when there is no PMC device installed.

3.5 Backup Battery

An onboard 3.6V lithium battery is provided to back up BIOS setup values and the real time clock (RTC). When replacing, the battery must be connected as follows:

1. Place your index and thumb at each side of the battery and gently pull out the battery.
2. Insert a new one firmly in place with respect to the positive and negative location of the pins.



WARNING

There is a danger of explosion if you replace the battery incorrectly.
Replace the battery with the same or equivalent type recommended by the manufacturer.
Dispose of used batteries according to the manufacturer's instructions.

3.5.1 Operation and Preventative Maintenance

The operational battery voltage must be between 2.9 and 3.6 volts.
When the board is stored and is kept in it's original package, the battery must be replaced when the battery voltage is below 2.9 volts.
For preventive operational maintenance, we recommend to verify the battery voltage after 4 years. After that period, we recommend that the safety voltage is checked more often. The normal battery life expectancy depends on the utilisation of the board.

- Kontron ordering MRP: 100-001
- Tadiran ordering MRP: 15-51-86-420-007 (TL-5186)

3.6 Board Hot Swap and Installation

Because of the high-density pinout of the hard-metric connector, some precautions must be taken when connecting or disconnecting a board to/from a backplane:

1. Rail guides must be installed on the enclosure to slide the board to the backplane.
2. Do not force the board if there is mechanical resistance while inserting the board.
3. Screw the frontplate to the enclosure to firmly attach the board to its enclosure.
4. Use extractor handles to disconnect and extract the board from its enclosure.

Note:
Hot swap of the CP6011 in a system slot is not defined. This results in a cold start of the system.

WARNING

Always use a grounding wrist wrap before installing or removing the board from a chassis.

WARNING

Removing the system host in a running system can harm some PCI I/O devices because the bus remains floating. At least, PCI reset should stay asserted, but not all systems detect this condition and hold reset active when no system slot is present.

CAUTION

In a system slot, the VIO must be set to 3.3V or 5V (Depending on Board Options), There is no limitation in a peripheral slot

3.6.1 Installing the Card in the Chassis

To install a card in a chassis:

1. Remove the filler panel of the slot or see “Removing the Card” below.
2. Ensure the board is configured properly.
3. Carefully align the PCB edges in the bottom and top card guide.
4. Insert the board in the system until it makes contact with the backplane connectors.
5. Using both ejector handles, engage the board in the backplane connectors until both ejectors are locked.
6. Fasten screws at the top and bottom of the faceplate.

3.6.2 Removing the Board

If you would like to remove a card from your chassis please follow carefully these steps:

1. Unscrew the top and the bottom screw of the front panel.
2. Push the red handle latch until the ejector fall free.
3. Using both ejectors, disengage the board from the backplane.
4. Pull the board out of the chassis.

3.6.3 Installing a PMC Card

To install a PMC card:

1. Remove the front bezel.
2. Carefully push the PMC to mate the four connectors.
3. Screw the four screws at the bottom of the PMC to fix it to the board.

WARNING

- The CompactFlash and the PMC B can not be used simultaneously.
- The IDE Mezzanine and the PMC B can not be used simultaneously.

3.6.4 Installing the IDE Mezzanine

To install the IDE mezzanine:

1. Carefully connect the IDE connector of the mezzanine to the IDE connector (J14) of the board.
2. Screw the four screws at the bottom of the PMC to fix it to the board.

3.6.5 Installing a CompactFlash

This product supports all type I and type II CompactFlash modules.

WARNING

Never install or remove the compact flash while the board is on.

To install the CompactFlash:

1. Remove the plastic retainer.
2. Insert the CompactFlash in place.
3. Reinstall the plastic retainer.

To remove the CompactFlash:

1. Remove the plastic retainer.
2. Pull the CompactFlash module out.
3. Install a new CompactFlash module.
4. Reinstall the plastic retainer

4. Building a cPCI System

Contents

4.1 Building a cPCI System

The basic components needed to build a CompactPCI system include:

- Chassis
- Backplanes
- Power supplies
- Ventilation unit
- System, peripheral or busless boards following application requirements
- Other accessories such as storage modules, Ethernet switches, system management cards, and RTM

See your system's manual for more details.

4.1.1 Backplane

The CP6011 is fully compatible with the XL-PSB, XL-LP41, XL-LP42 and XL-VHDS.
If using a third party system, consult you system's manual determine the system's compatibility with the CP6011.

J1 and J2 connectors must be compatible with PICMG2.0R3.0

Note:
J1 and J2 are de-facto industry standard as defined by PICMG2.0R3.0. The J3 connector is user defined. Pinouts vary from vendor to vendor. Backplanes should be feed-through with the exception of PICMG2.16R1.0 compliant system, which routes Ethernet signals into the backplane. J4 and J5 are defined by users and vary from vendor to vendor and should be feed-through. Systems that do not meet this requirement may permanently damage the CP6011. Contact Kontron Technical Support to verify pinout compatibility with other chassis backplanes.

4.1.2 Rear-Panel I/O

This feature is intended to issue the I/O capabilities of the CP6011 to the rear of the enclosure using a RTM I/O (cTM80-2).
The RTM I/O module gathers all the I/O signals of the CPU board and makes them easily accessible through standard headers and connectors located at the rear of enclosure. For more information about the cTM80-2 transition module, please consult our web site at: www.kontron.com

Note:
The CP6011 can detect older RTMs such as the cTM80-2, which forces the CP6011 to remain off. This protection only works with older RTMs from Kontron Canada.

WARNING

Always used the right RTM with your front board or permanent damage could occur

Note:
For most PICMG2.16 systems (XL-PSB and XL-LP42), you need to use a special RTM. The limitation does not apply to the XL-VHDS.

4.1.3 Storage Devices

The CP6011 can support a CompactFlash connected to the system processor through a T069. If more storage devices or DVD/floppy drives are needed, 6U form factor storage modules are supported with the XL-VHDS system. 3U SCSI trays also are supported in VHDS for very high storage capacity and very high MTBF. This requires a SCSI PMC. Consult you system's manual for available storage device.

4.1.4 Power Supply

Use of 3U or 6U Compact PCI power supplies is strongly recommended with the CP6011. Although you can use other power supply types, make sure they can handle the power requirement, current transient, and voltage tolerance. Use of an ATX power supply is not recommended.
3U and 6U CompactPCI power supply modules feature load sharing redundant mode and hot-swap capabilities, which allow on-site replacements of defective modules while the system remains on.

4.1.5 Connector Keying

CompactPCI connectors support guide lugs to ensure a correct polarized mating. A proper mating is enhanced by the use of color-coded keys for 3.3V and 5V operation. Color-coded keys prevent inadvertent installation of a 5V peripheral/system board in a 3.3V slot.
In peripheral mode, the CP6011 is universal in this respect, so there is no color key in J1. However, always key backplanes in accordance to their VIO settings. Note that 5V signaling forces a 33MHz PCI bus mode. When operating at 3.3V, all PCI and PCI-X frequencies are valid.
In system mode, the CP6011 is 3.3V or 5V (Depending on Option) only due to the CPCI bus pull-up values. To use the board with a 3.3V or 5V VIO you have to use correct board option.

Signaling Voltage	Key Color
3.3V	Cadmium Yellow
5V	Brilliant Blue
Universal board (5V and 3.3V)	None

Keying also is defined in the J4 connector to determine its usage. CP6011 supports user I/O on J4 so it is keyed with the nut-brown key. Backplanes that feed through J4 also have a brown key. Other J4 usages have their key defined in PICMG2.10R1.0.

J4 Usage	Key Color
User I/O	Nut Brown
H.110	Strawberry Red
Standard switch	Blue Lilac
Extended switch	Ocher Yellow

Cavity keying within the card guide and handle is used to protect J2, J3 and J5 usage. The CP6011 is keyed accordingly to PICMG2.10R1.0 and PICMG2.16R1.0. Few systems support this keying so you must take care to verify the type of slot before installing the board. XL-VHDS features complete keying and offers the greatest protection against pinout mismatch.

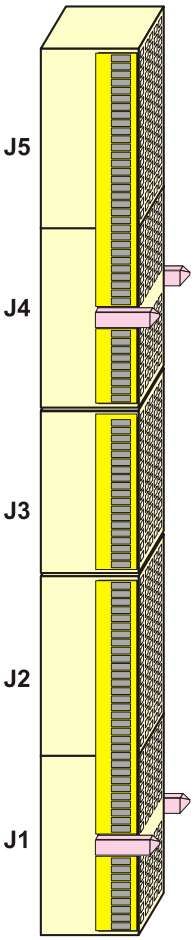
4.1.6 Bus Mastering

The CP6011 provides seven pairs of REQ/GNT (0-6) # arbitration signals through the secondary PCI bus. This means that the board can drive up to seven CPCI slots with PCI bus master capabilities.

CPCI I/O Signals

This section describes integrated feature signals available on rear panel CPCI I/O connectors (J3, J4, and J5).

4.1.7 CompactPCI Connectors



- **cPCI J5 Connector**

  Legacy connections (IDE, Floppy)

- **cPCI J4 Connector**

  SCSI Ultra-160 connections (SCSI board version)
  or PIM connections (PIM board version)

- **cPCI J3 Connector**

  LAN2 and LAN1, Serial Ports 1 and B, PS/2 Keyboard and Mouse, VGA, POST, ID, Speaker, and USB.

- **cPCI J2 Connector**

  64-bit extension, arbitration, clocks, reset, and power.

- **cPCI J1 Connector**

  Supports cPCI bus signals and power.

4.2 cPCI I/O Signals

4.2.1 J3 Signal Specification

4.2.1.1 Ethernet LAN 1 and LAN2

Signal	Pin Assignment	Description
LAN2, 1:ACT#	A13, B13, D13	Transmit / receive activity LED signal
LAN2, 1:LINK#	A14, B14, D14	Link integrity LED signal
LAN:CT	C14	

Signal	Pin	Signal	Pin
LAN2:DA+	A18	LAN1:DA+	A16
LAN2:DA-	B18	LAN1:DA-	B16
LAN2:DB+	A17	LAN1:DB+	A15
LAN2:DB-	B17	LAN1:DB-	B15
LAN2:DC+	D18	LAN1:DC+	D16
LAN2:DC-	E18	LAN1:DC-	E16
LAN2:DD+	D17	LAN1:DD+	D15
LAN2:DD-	E17	LAN1:DD-	E15

4.2.1.2 Serial Port 0 (COM1)

Signal	Pin Assignment	Description
COM1:DCD	D1	Data Carrier Detect
COM1:RXD	B1	Receive Data
COM1:DSR	C1	Data Set Ready
COM1:TXD	D2	Transmit Data
COM1:RTS	A1	Ready To Send
COM1:CTS	C2	Clear To Send
COM1:RI	A2	Ring Indicator
COM1:DTR	B2	Data Terminal Ready

4.2.1.3 Serial Port 1 (COM2)

Signal	Pin Assignment	Description
COM2:DCD	D3	Data Carrier Detect
COM2:RXD	B3	Receive Data
COM2:DSR	C3	Data Set Ready
COM2:TXD	D4	Transmit Data
COM2:RTS	A3	Ready To Send
COM2:CTS	C4	Clear To Send
COM2:RI	A4	Ring Indicator
COM2:DTR	B4	Data Terminal Ready

4.2.1.4 USB0, USB1

Signal	Pin Assignment	Description	
USB0:DATA+-, DATA-	B8, A8	USB Data	Differential data path for USB 0 port
USB1:DATA+, DATA-	B9, A9	USB Data	Differential data path for USB 1 port
USB0,1:VCC	B10, A10	USB Voltage	Differential power level for USB 0 and 1 port

4.2.1.5 Keyboard

Signal	Pin Assignment	Description
KB:DATA	E4	Keyboard Data
KB:CLK	E5	Keyboard Clock

4.2.1.6 Mouse

Signal	Pin Assignment	Description
MOUSE:DATA	E3	Mouse Data
MOUSE:CLK	E2	Mouse Clock

4.2.1.7 Speaker

Signal	Pin Assignment	Description
SPEAKER	E7	Speaker signal

4.2.1.8 POST

Signal	Pin Assignment	Description
POST:DATA	E6	POST data
POST:CLK	D6	POST clock

4.2.1.9 Video

Signal	Pin Assignment	Description
VGA:HSYNC	B5	Horizontal synchronization
VGA:VSYNC	C5	Vertical synchronization
VGA:SCLK	D5	Video serial clock line
VGA:SDATA	C6	Video serial data line
VGA:RED	A6	Analog red video signal
VGA:GREEN	B6	Analog green video signal
VGA:BLUE	A5	Analog blue video signal

4.2.1.10 ID

Signal	Pin Assignment	Description
ID1 – ID4	E1, B7, C7, D7	

4.2.1.11 Power

Signal	Pin Assignment	Description
VCC	A19, B19	+5V Supply voltage
VCC3	C19	+3.3V Supply voltage
+12V	D19	+12V Supply voltage
-12V	E19	-12V Supply voltage
GND	C15 - C18	Ground

4.2.1.12 ID

Signal	Pin Assignment	Description
RSV	A11, A12, B11, B12, C8-C13, D8-D14, E8-E14	Reserved for Kontron internal use.

4.2.2 J4 Signal Specification

4.2.2.1 SCSI Interface

Signal	Pin Assignment	Description
D0+ to D15+	D4, A5, D5, A7, D7, A8, D8, A10, A24, D24, D22, D25, A1, D1, A2, D2	SCSI data.
D0- to D15-	E4, B5, E5, B7, E7, B8, E8, B10, B24, E24, B25, E25, B1, E1, B2, E2	The SCSI data lines drive the ID during arbitration and selection, and command and data information as well as status and messages.
TERMPWR1 to TERMPWR9	A16,B16, A15, B15, D15, E15, B11, D11, E11	Termination power.
IO +/-	D22, E22	In/Out – Indicates the in direction when asserted and the out direction when not asserted.
REQ + / -	A22, B22	Request – A target will assert REQ to indicate a byte is ready or is needed by the target.
CD + / -	D21, E21	Command/Data – Indicates Command or message phase when asserted, and data phase when not asserted.
SEL + / -	A21, B21	SCSI Select – The line is driven after a successful arbitration to select as an initiator or reselect as a target and otherwise it is received.
MSG + / -	D19, E19	SCSI Message - Indicates a message phase when asserted, and command or data phase when not asserted.
RST + / -	A19, B19	Reset – Signal is interpreted as a hard reset and will clear all commands pending on the SCSI bus.
ACK +/-	D18, E18	Acknowledge – Indicates a byte is ready for or was received from the target.
BSY + / -	A18, B18	Busy – Handshake signal used during arbitration.
ATN + / -	D16, E16	Attention – This line is activated when a special condition occurs.
DPL + / -	D10, E10	SCSI High Parity – Provide odd parity for data lines
DPH + / -	A4, B4	SCSI Low Parity – Provide odd parity for data lines.
DIFFSENS	A11	Differential Sense Detects the voltage level of a SCSI signal to determine whether it is a single-ended or LVD.
VCC	B23	+5V
VCC3	E23	+3.3V
GND	A3, A6, A9, A17, A20, B3, B6, B9, B17, B20, C1 to C25, D3,D6,D9, D17, D20, E3, E6,E9, E17, E20	Ground
RSV	A23, D23	Reserved for Kontron internal use.

4.2.2.2 PIM Interface

Signal	Pin Assignment	Description
PIM1 to PIM 10	A25, D25, B25, E25, A24,D24, B24, E24, A22, D22	PIM Interface
PIM11 to PIM20	B22, E22, A21, D21, B21, E21, A19, D19, B19, E19	
PIM21 to PIM30	A18, D18, B18, E18, A16, D16, B16, E16, A15, D15	
PIM31 to PIM40	B15, E15, A11, D11, B11, E11, A10,D10, B10, E10	
PIM41 to PIM50	A8, D8, B8, E8, A7,D7, B7, E7, A5, D5	
PIM51 to PIM60	B5, E5, A4, D4, B4, E4, A2, D2, B2, E2	
PIM61 to PIM64	A1, D1, B1, E1	
VCC	B23	+5V
VCC3	E23	+3.3V
GND	A3, A6, A9, A17, A20, B3, B6, B9, B17, B20, C1 to C25, D3,D6,D9, D17, D20, E3, E6,E9, E17, E20	Ground

4.2.2.3 Mezzanine Connector (JN4)

Signal	Pin Assignment	Description
P1+ to P32+	1, 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30, 33, 34, 37, 38, 41, 42, 45, 46, 49, 50, 53, 54, 57, 58, 61, 62	
P1- to P32-	3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28, 31, 32, 35, 36, 39, 40, 43, 44, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64	

4.2.3 J5 Signal Specification

4.2.3.1 IDE Interface

Signal	Pin Assignment	Description
IDE:RESET#	E15	Reset signal
IDE1:D0-D15	A18, D18, A17, D17, A16, D16, A15, D15, B15, E16, B16, E17, B17, E18, B18, E19,	Disk Data – These signals are used to transfer data to or from the IDE device.
IDE1:DMARQ	D19	Disk DMA Request - This signal is directly driven from the IDE device DMARQ signal. It is asserted by the IDE device to request a data transfer.
IDE1:IOW#	B19	Disk I/O Write – In normal IDE mode, this is the command to the IDE device that it may latch data from data lines.
IDE1:IOR#	A19	Disk I/O Read – In normal IDE mode, this is the command to the IDE device that it may drive data on SDD lines.
IDE1:IORDY	E20	I/O Channel Ready –This input signal is negated to extend the host transfer cycle of any host register read/write access when the drive is not ready to respond to a data transfer request. When not negated, it is in a high impedance state.
IDE1:DMACK#	D20	DMA Acknowledge – This signal directly drives the IDE device /DMACK signal. It is asserted to indicate to IDE DMA slave devices that a given data transfer cycle is a DMA data transfer cycle.
IDE1:ACT#	A22	Activity indicator
IDE1:IRQ	B20	IRQ line
IDE1:IOCS16#	A20	I/O Chip Select - Indicates to the host that the 16-bit data port has been addressed and the drive is prepared to send/receive a 16-bit data word.
IDE1:A0 – A2	B21, D21, A21	Disk Address – These signals indicates which byte in either the ATA command block or control block is being addressed.
IDE1:CS0#, CS1#	D22, B22	Chip Select - For ATA control register
IDE1:PDIAG#	E21	Diagnostic - Will be asserted by Drive 1 to indicate to Drive 0 that it has passed diagnostics. Following a power-on reset or software reset, Drive 1 will negate -PDIAG within 1 msec to indicate to Drive 0 that it is busy.

4.2.3.2 *Floppy Disk Interface*

Signal	Pin Assignment	Description
FD:INDEX#	B11	Index
FD:MTR0,1#	A11, B12	Motor 0-1 enable
FD:DSEL 0,1#	D12, E12	Drive 0-1 select
FD:DIR#	A12	Direction
FD:STEP#	E13	Step pulse
FD:WDATA#	D13	Write disk data
FD:WGATE#	B13	Write gate
FD:TRK0#	A13	Track 0
FD:WRPROT#	E14	Write protected
FD:RDATA#	D14	Read disk data
FD:HDSEL#	B14	Head select
FD:DSKCHG#	A14	Disk change
FD:DENSEL#	E11	Also named DRVDEN0. Density select. Indicate the drive and media selected.
FD:MSEN0 FD:MSEN1	A10 B10	Automatic media sense
FD:FDEDIN#	D11	Also named DRVDEN1. Used along DENSEL. Indicates the drive and media selected.

4.2.3.3 *Ground and Reserved Pins*

Signal	Pin Assignment	Description
GND	Row C (C1-C22)	Ground
RSV	A1-A9, B1-B9, D1-D10, E1-E10, E22	Reserved for Kontron internal use.

5. Software Setup

Contents

5.1 PHOENIX BIOS Setup Program

All relevant information for operating the board and connected peripherals is stored in the CMOS memory. A battery-backed up memory holds this information when the board is powered off, the BIOS Setup program is required to make changes to the setup.

5.1.1 Accessing the BIOS setup program

The system BIOS (Basic Input Output System) provides an interface between the operating system and the hardware of the CP6011. The CP6011 uses the Phoenix Setup program, a setup utility in flash memory that is accessed by pressing the <DELETE> key at the appropriate time during system boot. This utility is used to set configuration data in CMOS RAM.

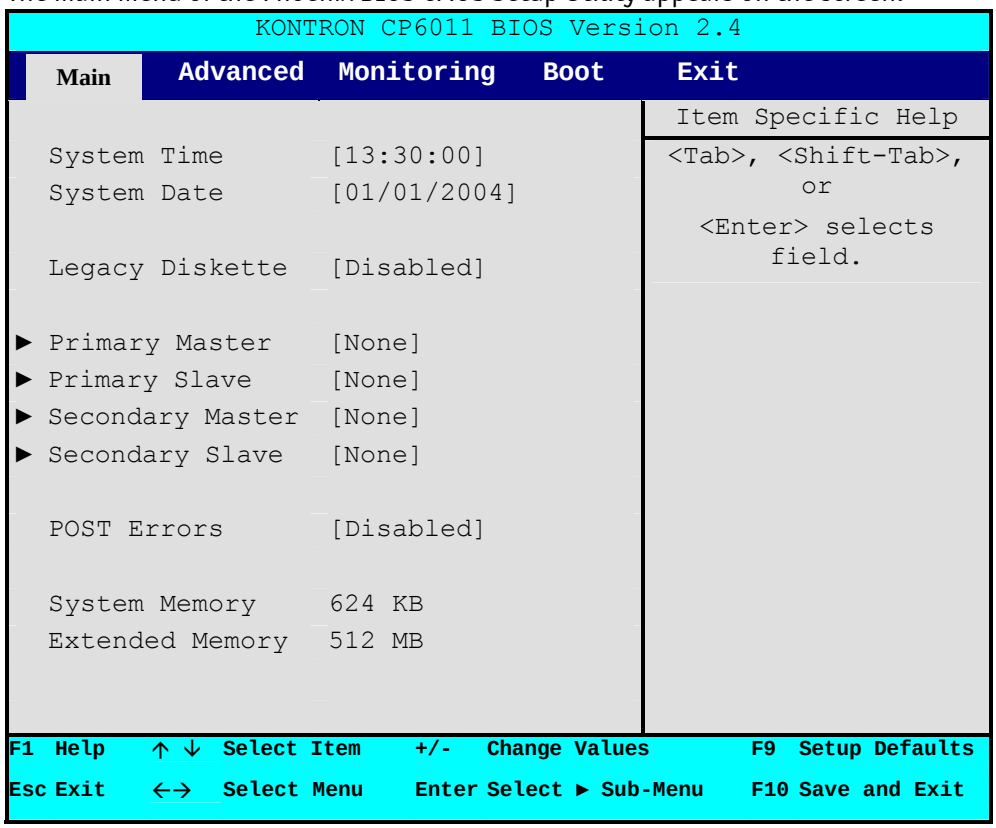
To run the Phoenix Setup program incorporated in the ROM BIOS:

- Turn on or reboot the system.
- When you get the following message, hit <DELETE> key to enter SETUP

PhoenixBIOS 4.0 Release 6.0
Copyright 1985-2002 Phoenix Technologies Ltd.
All Rights Reserved

KONTRON CP6011 BIOS Version 2.4

The main menu of the Phoenix BIOS CMOS Setup Utility appears on the screen.



Whenever you are not sure about a certain setting, you may refer to the list of default values. The list of defaults is provided in the event that a value has been changed and one wishes to set this option to its original value. Loading the SETUP defaults will affect all parameters and will reset options previously altered.

The Setup Defaults values provide **optimum performance** settings for all devices and system features.

Note:

The CMOS setup option described in this section is based on **BIOS Version 2.4**. The options and default settings may change in a new BIOS release.

CAUTION

These parameters have been provided to give control over the system. However, the values for these options should be changed only if the user has a full understanding of the timing relationships involved.

5.1.2 The Menu Bar

The Menu Bar at the top of the window lists these selections:

Menu selection	Description
Main	Use this menu for basic system configuration.
Advanced	Use this menu to set the Advanced Features available on your system.
Monitoring	Use this menu to configure Monitoring features.
Boot	Use this menu to determine the booting device order.
Exit	Use this menu chose Exits option.

Use the left and right ← and → arrows keys to make a selection.

5.1.2.1 The Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The chart on the following page describes the legend keys and their alternates:

Key	Function
<F1> or <Alt-H>	General Help windows
<Esc>	Exit this menu.
← → arrow keys	Select a different menu
<Home> or <End>	Move cursor to top or bottom of window.
<PgUp> or <PgDn>	Move cursor to top or bottom of window.
<F5> or <->	Select the Previous Value for the field.
<F6> or <+> or <Space>	Select the Next Value for the field.
<F9>	Load the Default Configuration values for all menus
<F10>	Save and exit.
<Enter>	Execute Command, display possible value for this field or Select the Sub menu

To select an item, use the arrow keys to move the cursor to the field your want. Then use the plus-and-minus value keys to select a value for that field. To save values commands in the Exit Menu save the values currently displayed in all the menus.

To display a sub-menu, use the arrow keys to move the cursor to the sub menu your want. Then press <Enter>. A pointer (▶) marks all sub menus.

5.1.2.2 The Field Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field.

5.1.2.3 The General Help Windows

Pressing <F1> or <Alt-H> on any menu brings up the General Help window that describes the legend keys and their alternates:

General Help

Setup changes system behavior by modifying the BIOS configuration. Selecting incorrect values may cause system boot failure; load Setup Default values to recover.

<Up/Down> arrows select fields in current menu.
<PgUp/PgDn> moves to previous/next page on scrollable menus.
<Home/End> moves to top/bottom item of current menu.

Within a field, <F5> or <-> selects next lower value and <F6>, <+>, or <Space> selects next higher value.

<Left/Right> arrows select menus on menu bar.
<Enter> displays more options for items marked with ▶.

<F9> loads factory installed Setup Default values.
<F10> saves current settings and exits Setup.

<Esc> or <Alt-X> exits Setup; in sub-menus, pressing these keys returns to the previous menu.

<F1> or <Alt-H> displays General Help (this screen).

[Continue]

5.1.2.4 *Main Menu Selection*

The scroll bar on the right of any windows indicates that there is more than one page of information in the windows. Use <PgUp> and <PgDn> to display all the pages. Pressing <Home> and <End> displays the first and last page. Main Menu Selection
You can make the following selections on the Main Menu itself. Use the sub menus for other selections.

Feature	Options			Description
System Time	HH:MM:SS			Set the system time.
System Date	MM/DD/YYYY			Set the system date.
Legacy Diskette A:	Disabled 1.44/1. 25 MB 3 ½"			Select the type of floppy disk drive installed in your system. **Note:** 1.25MB 3 ½" references a 1024 byte/sector Japanese media format. The 1.25MB, 3 ½ diskette requires a 3-Mode floppy-disk drive.
Primary Master	Type	None		None: No booting device installed.
		CD-ROM	Multi-Sector Transfers	**Multi-Sector Transfers** Choices: Disabled, 2,4,8, and 16 sectors Any selection except Disabled determines the number of sectors transferred per block. Standard is 16 sectors per block.
			LBA Mode Control	**LBA Mode Control** Choices: Disabled, Enabled Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, heads, and Sectors.
			32 BIT I/O	**32 Bit I/O** Choices: Disabled, Enabled Enables 32-bit communication between CPU and IDE card. Requires PCI or local bus.
			Transfer Mode	**Transfer Mode** Choices: Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPIO 3 / DMA 1, FPIO 4 / DMA2. Selects the method for transferring the data between the hard disk and system memory. The Setup menu only lists those options supported by the drive and platform.
			Ultra DMA Mode	**Ultra DMA Mode** Choices: Disabled, Mode 0, 1, 2, 3, 4, 5. Select the Ultra DMA mode used for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
			SMART Monitoring	**SMART Monitoring** Display type of Monitoring. This field is a "Display Only". This option can be changed in the Advanced Menu.
		ATAPI Removable		Same choices as CD-ROM

Main Menu Selection (continued)

Feature	Options			Description
Primary Master (Continued)	Type (continued)	IDE Removable		Same choices as CD-ROM
		Other ATAPI		Same choices as CD-ROM
		(USER)	Cylinders	**Cylinders** Set the number of cylinders
			Heads	**Heads** Set the number of heads. Choices are 1 to 16
			Sectors	**Sectors** Set the number of sectors per track
			Maximum Capacity	**Maximum Capacity** Maximum capacity is displayed according to the cylinders, heads and sectors selected.
			Multi-Sector Transfers	**Multi-Sector Transfers** Choices are: Disabled, 2, 4, 8 and 16 sectors. Specify the number of sectors per block for multiple sector transfers. "MAX" refers to the size the disk returns when queried.
			LBA mode Control	**LBA Mode Control** Choices are: Enabled, Disabled Enabling LBA cause Logical Block Addressing to be used in place of Cylinders Heads and Sectors
			32 Bit I/O	**32 Bit I/O** Choices are: Enabled, Disabled. This setting enables or disables 32 bit IDE data transfers.
			Transfer Mode	**Transfer Mode** Choices are: Standard, Fast PIO 1, Fast PIO 2, Fast PIO 3, Fast PIO 4, FPIO 3 / DMA 1, FPIO 4 / DMA2. Select the method for moving data to/from the drive. Autotype the drive to select the optimum transfer mode.
			Ultra DMA Mode	**Ultra DMA Mode** Choices are: Disabled, Mode 0 to 5. Select the Ultra DMA mode used for moving data to/from the drive Autotype the drive to select the optimum transfer mode.
			SMART Monitoring	**SMART Monitoring** IDE Failure Prediction
		Auto		BIOS auto detects the hard disk installed
Primary Slave				Same as Primary Master
Secondary Master	Same as Primary Master			
Secondary Slave	Same as Primary Master			
POST Errors	Enabled Disabled			Pauses and displays SETUP entry or resumes boot prompt if error occurs on boot. If disabled, system always attempts to boot.
System Memory	N/A			Displays amount of conventional memory detected during boot up.
Extended Memory	N/A			Displays the amount of RAM memory detected during boot up minus the base memory (1 Mbyte).

5.1.2.5 *Advanced Menu Selection*

You can make the following selections on the Advanced Menu. Use the sub menus for other selections.

Feature	Options	Description
Boot Settings Configuration	This is a Sub-Menu	Additional setup menus to configure boot settings.
PCI Configuration	This is a Sub-Menu	Additional setup menus to configure PCI devices
On-Board Device Configuration	This is a Sub-Menu	Peripheral Configuration
Advanced Chipset Control	This is a Sub-Menu	Select options for Advanced Chipset features.
Console Redirection	This is a Sub-Menu	Additional setup menus to configure console.
Advanced Processor Options	This is a Sub-Menu	Select options for Advanced Processor specific options.

5.1.2.5.1 Boot Settings Configuration

Feature	Options	Description
Installed O/S	Other Win2000	Other : General Settings Win2000: Specific Settings **Note:** An incorrect setting can cause some operating systems to display unexpected behavior.
Enable ACPI	Yes No	Enable/Disable ACPI BIOS (Advance Configuration and Power Interface)
Reset Configuration Data	No Yes	Select "Yes" if you want to clear the Extended System Configuration Data (ESCD) area.
Boot-time Diagnostic Screen	Enabled Disabled	Displays the Diagnostic Screen during Boot. Always Enabled when Console Redirection is activated.
Extended Memory Testing	Normal Just zero it None	Determines which type of test will be performed on extended memory (above 1M).
Summary Screen Delay	None 5 seconds	Delay to display the system configuration at boot time.
Save CMOS in FLASH	Disabled Enabled	Saving CMOS memory content into Flash Memory will prevent loosing CMOS options when battery fails.
Retry Boot Sequence	Disabled Enabled	Enable this option to Retry the Boot sequence until a successful boot. (infinite Retry)
PS/2 Mouse	Disable Enabled	'Disabled' prevent any installed PS/2 mouse from functioning, but frees up IRQ 12. 'Enabled' forces the PS/2 mouse port to be enabled regardless if a mouse is present.
SMART Device Monitoring	Disabled Enabled	IDE Failure Prediction
Floppy check	Disabled Enabled	Enabled verifies floppy type on boot; disabled speed boot.

5.1.2.5.2 PCI Configuration

Feature	Options	Description
On-board Ethernet Controller	This is a Sub-Menu	Additional setup menus to configure On-board Ethernet Controller.
On-board PMC Expansion	This is a Sub-Menu	Additional setup menus to configure PMC Expansion Slot.
PCI Performance Settings	This is a Sub-Menu	Additional setup menus to configure PCI Performance settings.
Default Primary Video Adapter	External On-board	Select "External to have a PCI video card (must be installed) to be set as the Boot Display Device. Select "On-board" to have the On-Board video controller as the Boot Display Device.
Delay before PCI Initialization	0 to 7	Delay in seconds before PCI Initialization. Some external cards may require a minimum delay after reset before they can be accessed. Cards with onboard CPU that emulate a PCI Controller (ex.: RAID) are more likely to require a delay.
IDE – Device 31, Function 1	Enabled Disabled	Enabled or Disabled the IDE controller.
Legacy USB Support	Enabled Auto	Enables support for Legacy Universal Serial Bus.

5.1.2.5.2.1 On-board Ethernet Controller

Feature	Options	Description
Onboard Ethernet Controller 1	Enabled Disabled	Enables/Disables Onboard Gigabit Ethernet Controller (i82544) on Bus B, Device 00.
Option ROM	Enabled Disabled	Initialize device expansion ROM.
Onboard Ethernet Controller 2	Enabled Disabled	Enables/Disables Onboard Gigabit Ethernet Controller (i82544) on Bus B, Device 01.
Option ROM	Enabled Disabled	Initialize device expansion ROM.
Onboard Ethernet Controller 3	Enabled Disabled	Enables/Disables Onboard 10/100 Ethernet Controller (i82551er) on Bus D, Device 06.
Option ROM	Enabled Disabled	Initialize device expansion ROM.

5.1.2.5.2.2 On-board PMC Expansion

Feature	Options	Description
On-board PMC A Expansion Slot		
Option ROM scan	Enabled Disabled	Initialize device expansion ROM.
Latency Timer	Default, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allotted for bus master in units of PCI bus clocks.
On-board PMC B Expansion Slot		
Option ROM scan	Enabled Disabled	Initialize device expansion ROM.
Latency Timer	Default, 0020h, 0040h, 0060h, 0080h, 00A0h, 00C0h or 00E0h	Minimum guaranteed time slice allotted for bus master in units of PCI bus clocks.

5.1.2.5.2.3 PCI Performance settings

Feature	Options	Description
PCI Cache Line Size	0, 1,2, 4, 8 or 16 DWORDS	Set the Cache Line Size in DWORDS. Sets the Cache Line Size Register in the Configuration Space of PCI devices.
Onboard HB8 PCI-X Bridge settings:		Title for next options.
Force 64-bit Control	Disabled Both Secondary Primary	32-bit Prefetchable reads or 32-bit Posted Memory Write cycles on one side will be converted to 64-bit cycles on completion to target side if target supports 64-bit transfers.
Smart Prefetch Mechanism	Enabled Disabled	After a prefetch command, the remaining prefetched data will NOT be discarded, but will be available for the next Read Command with consecutive address.
Smart Prefetch Timeout	32 PCICLK 64 PCICLK 128 PCICLK 256 PCICLK	When Smart Prefetch is Enabled, the prefetched data is only discarded upon a Timeout.
Prefetching scheme	By EEPROM Aggressive Normal Manual	Controls Secondary PCI bus Prefetch behaviour (no effect when in PCI-X mode). If set to 'By EEPROM', the values shown are taken from the Bridge and are not available for change. This happens if a valid EEPROM content is detected and were loaded by the Bridge. The default aggressive Prefetching may affect the overall performance with some PCI Masters that cannot prefetch a lot of data due to limited buffers size or other reasons. If set to 'Manual', the options can be changed for optimum performance, which depends on the PCI device(s) present.
PCIX Primary Initial Prefetch count	1 2 4 8 16	Controls initial Prefetch Cache Lines count on the Primary bus during reads to prefetchable memory space. This value defines the cache line multiples for the initial prefetch count.
PCI Sec. Initial Prefetch count	8 16 32 Dwords	Controls initial Prefetch Dwords count on the Secondary bus during reads initiated from the primary port (no effect when in PCI-X mode).
PCI Sec. Incremental Prefetch count	None 4 8 12 16 20 24 28 32 Dwords	Controls Incremental Read Prefetch Dwords count. When an entry's remaining Prefetch Dword count falls below this value, the bridge will prefetch an additional "PCI Sec. Incremental Prefetch count" Dwords (no effect when in PCI-X mode). The count must not exceed half the value in the "PCI Sec. Maximum Prefetch count". Otherwise, no Incremental Prefetch will be performed.

PCI Sec. Maximum Prefetch count	(2 to 64 Dwords) 2 3 30 32 34 63 64	Controls the maximum count of prefetcheable Dwords that are allocated to one entry on the Secondary when flow through for that entry was not achieved (no effect when in PCI-X mode). Exception: 0 = 256 bytes (64 Dwords) = maximum programmable count.

5.1.2.5.3 On-board Device Configuration

Feature	Options	Description
Serial port A	Enabled Disabled Auto	Configure serial port A using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Base I/O address	3F8 2F8 3E8 2E8	Sets the base I/O address for serial port A.
Interrupt	IRQ 4 IRQ3	Sets the interrupt for serial port A.
Serial port B	Enabled Disabled Auto	Configure serial port B using options: **Disabled :** No configuration **Enabled :** User configuration **Auto :** BIOS or OS chooses configuration
Base I/O address	3F8 2F8 3E8 2E8	Sets the base I/O address for serial port B.
Interrupt	IRQ4 IRQ3	Sets the interrupt for serial port B.
Mode	RS-422 RS-485 RS-232	Set the mode for Serial Port B.
Floppy Disk Controller	Enabled Disabled Auto	Enables the Floppy Disk Controller.

5.1.2.5.4 Advanced Chipset Control

Feature	Options	Description
ECC Config	Disabled ECC	If enabled, BIOS will initialize ECC. This will lengthen POST time execution.

5.1.2.5.5 Console Redirection

Feature	Options	Description
Console Redirection	Disabled Enabled	If enabled, Console Redirection works without the VT100 jumper to use the console Redirection. This option is only used when jumper is not present.
Com Port Address	On-board COMA On-Board COMB	If enabled, it will use a port on the motherboard. Install the VT100 jumper to use the Console Redirection using the selected port.
Baud Rate	300, 1200, 2400, 9600, 19.2K, 38.4K, 57.6K, 115.2K	Enables the specified baud rate.
Parity		Fix setting: No Parity
Data Bits		Fix setting: 8 Data Bits
Stop Bit(s)		Fix setting: 1 Stop Bit
Console Type	VT100 VT100, 8bit PC ANSI, 7bit PC ANSI VT100+ VT-UTF8	Enables the specified console type.
Flow Control	None XON/XOFF CTS/RTS	Enables Flow Control.
Continue C.R. after POST	Off, On	Enables Console Redirection after OS has loaded.

5.1.2.5.6 Advanced Processor Options

Feature	Options	Description
Speed Step Support	POM BOM	BOM: Battery Optimized Mode (low power, low frequency). POM: Performance Optimized Mode (high power, high frequency).

5.1.2.5.7 Monitoring Menu

Feature	Options	Description
Intelligent System Monitoring	This is a Sub-Menu	
IPMI System Management OR BMC Device is not available	This is a Sub-Menu	NOTE: the sub-menu is not available if the BMC Reset jumper is installed (W9). The BIOS Setup will in that case show: Check the BMC reset jumper and the IPMI Firmware version update.
IDE Activity LED	IDE Activity IPMI Activity	Set IDE Activity Led usage.
Watchdog After POST	Enabled Disabled	Enables the Watchdog circuit after the POST sequence. Application software must refresh the Watchdog to prevent System Reset.
Watchdog Duration	16 seconds 1 minute 4 minutes	Select the duration time of the Watchdog timing circuitry.
FPGA IRQ	IRQ 5 IRQ 7 Disabled	Select FPGA IRQ for SWITCH, WATCHDOG and ENUM# events. If '*' is shown, this IRQ# is already used by KCS-SMS IRQ.
Automatic TCC	Enabled Disabled	This enables or disables the Intel processor Automatic Thermal Control Circuit (TCC). When enabled, the processor clock will be forced to a 50% duty cycle if the internal temperature exceeds its limit.
Delay prior to enabling the TCC	Disabled 2 Minutes 4 Minutes 8 Minutes 16 Minutes 32 Minutes	The Thermal Control Circuit (TCC) must be disabled just prior to transferring control to the operating System. This is necessary in order for the Operating System's timing calibration to complete accurately. This delay is valid for both Automatic and OnDemand TCC.

5.1.2.5.8 Intelligent System Monitoring

Feature	Options	Description
Interrupt Generation	Enabled Disabled	Enables/disables the generation of interrupts when an event occurs. This must be set to Disabled when programs such as LANDesk(R) are loaded onto the system.
Hardware Monitor Temperature	This is a Sub-Menu	
Hardware Monitor Voltage Inputs	This is a Sub-Menu	
Control Temperature Events	This is a Sub-Menu	
Control Voltage Events	This is a Sub-Menu	

5.1.2.5.8.1 Hardware Monitor Temperature

Feature	Options	Description
CPU Die Temperature	Display a Status.	The following are temperature at the various sensors present on the board. Please refer to manual for location of those sensors.
Board Sensor A (Q1)	Display a Status.	
Board Sensor B (Q2)	Display a Status.	

5.1.2.5.8.2 Hardware Monitor Voltage Inputs.

Feature	Options	Description
Vcore	Displays a Status.	When enabled, events can be triggered when a specific voltage cross below the LoLimit or above the HiLimit. The following is the different voltage usage on the board: 1.25V → Memory 3.3V → Misc. 5V → Misc. +- 12V → Misc. 1.05V → Chipset & CPU Vbat → Battery (RTC)
Vin 1.25V	Displays a Status and limits set in other menu	
Vin 3.3V	Displays a Status and limits set in other menu	
Vin 5V	Displays a Status and limits set in other menu	
Vin 12V	Displays a Status and limits set in other menu	
Vin -12V	Displays a Status and limits set in other menu	
Vin 1.05V	Displays a Status and limits set in other menu	
Vbat	Displays a Status and limits set in other menu	

5.1.2.5.8.3 Control Temperature Events

Feature	Options	Description
CPU Temperature Interrupt	Enabled Disabled	This option enables Temperature events handling.
Resume Alarm (oC)	10 to 70°C in 4°C increment	Full speed (Normal mode) will be resumed when the temperature comes down to the selected temperature.
Overheat Alarm (oC)	30 to 90°C in 4°C increment	The CPU will be slowed down (Doze mode) when it reaches the selected temperature.
On-Demand TCC Duty Cycle	Disabled 12.5% 25.0% 37.5% 50.0% 62.5% 75.0% 87.5%	This is the period in which the clock is running. Note that Automatic TCC has precedence if both Automatic and On-Demand TCC are enabled. Exemple: If 12.5% is selected the clock will run 12.5% of the overall time.

5.1.2.5.8.4 Control Voltage Events

Feature	Options	Description
Vin 1.25V Voltage Interrupt	Enabled Disabled	This option enables Temperature events handling.
Vin 3.3V Voltage Interrupt	Enabled Disabled	
Vin 5V Voltage Interrupt	Enabled Disabled	
Vin 12V Voltage Interrupt	Enabled Disabled	
Vin -12V Voltage Interrupt	Enabled Disabled	
Vin 1.05V Voltage Interrupt	Enabled Disabled	
Vbat Voltage Interrupt	Enabled Disabled	

5.1.2.5.9 IPMI System Management

Feature	Options	Description
IPMI Device and Firmware Information	**This is a Sub-Menu**	Intelligent Platform Management Interface (IPMI) information.
FRU Board Information	**This is a Sub-Menu**	Field Replaceable Unit (FRU) information about the board.
KCS-SMM SMI	Enabled Disabled	Allow Baseboard Management Controller (BMC) SMI handler for the initialization or startup of certain functions in the Management Controllers, such as setting the initial timestamp time. WARNING: option forced to Disabled if the TEST jumper is installed.
KCS-SMS IRQ	IRQ5 IRQ7 Disabled	Select BMC IRQ for the System Management Software (SMS). SMS takes platform management information and links it into other aspects of systems management, such as software management and distribution, alerting, remote console access, etc. If '*' is shown, this IRQ# is already used by FPGA IRQ.
Dual Port IPMB Redundancy	Enabled Disabled	Intelligent Platform Management Bus (IPMB). Enabled - IPMB1 is hidden behind IPMB0 and used as a Redundancy channel. Disabled - IPMB0 and IPMB1 operate as separate channels.
Management controller Configuration	Basebord Satellite	BMC - the board is the 'central' management controller. Satellite - the Board is a Satellite Management Controller, under the control of an external 'central' Management Controller. The BMC manages the interface between system management and the platform management hardware.
Clear SEL	No Yes	Select 'YES' if you want to clear all contents of the IPMI System Event Log on next boot only.
IPMI Watchdog Timer Use	None BIOS/POST OS Load Both	Indicates the current use assigned to the Watchdog Timer. BIOS/POST – Watchdog Timer used by the BIOS POST. OS Load - OS Load Timeout. This mode requires SMS or OS support.
BIOS Timer Countdown	30 sec, 1 min, 2 min or 4 min	Initial BIOS Timer Countdown Value.
OS Load Timer Countdown	30 sec, 1 min, 2 min, 4 min, 8 min, 16 min or 32 min	Initial OS Load Timer Countdown Value.
OS Load Timer Action	None Hard Rst Pwr Down Pwr Cycle	Initial OS Load timeout action. None - no action. Hard Reset. Power Down. Power cycle.

5.1.2.5.9.1 IPMI Device and Firmware Information

Feature	Static information	Description
Product ID	6011	Kontron board identifier. Provide a numeric value that identifies a particular System (or board) type.
IPMI Version	1.5	IPMI specification version. This field holds the version of the IPMI specification that the controller is compatible with.
Device ID	3	IPMI implementation ID used with this product ID. Provide a numeric value that identifies a particular controller type.
Device Revision	0	
Firmware Revision	3.02	IPMI firmware revision.
SDR Revision	7	Sensor Data Records package revision.
CPCI Slot Number	8	

5.1.2.5.9.2 FRU Board Information

Feature	Static information	Description
Board Product Number	CP6011	Inventory information about the board.
Board Serial Number	1000123456	
Board Part Number	T6011###A_1000	

5.1.2.5.10 Boot Menu

Feature	Options	Description
Boot Menu	Boot From Primary Master	
	Boot From Primary Slave	
	Boot From Secondary Master	
	Boor From Secondary Slave	
	Boot From Floppy	
	Boot From CDROM	
	Boot From CompactFlash	
	Boot From SCSI (External)	
	Boot From LAN1	
	Boot From LAN2	
	Boot From LAN3	
	Boot From USB CDROM	
	Boot From USB Floppy	

5.1.2.6 Exit Menu Selection

Feature	Options		Description
	Exit Saving Changes	Yes / No	**Exit Saving Changes** Setup and save your changes to CMOS.
	Exit Discarding Changes	Yes / No	**Exit Discarding Changes** Exit utility without saving Setup data to CMOS.
	Load Setup Defaults	Yes / No	**Load Setup Defaults** Load default values for all SETUP items.
	Discard Changes	Yes / No	**Discard Changes** Load previous values from CMOS for all SETUP items.
	Saves Changes	Yes / No	**Save Changes** Save Setup Data to CMOS.

5.1.3 Boot Utilities

Phoenix Boot Utilities are: Phoenix QuietBoot™
Phoenix MultiBoot™

Phoenix QuietBoot displays a graphic illustration rather than the traditional POST messages while keeping you informed of diagnostic problems.
Phoenix MultiBoot is a boot screen that displays a selection of boot devices from which you can boot your operating system.

5.1.3.1 Phoenix Quiet Boot

Right after you turn on or reset the computer, Phoenix QuietBoot displays the QuietBoot Screen, a graphic illustration created by the computer manufacturer instead of the text-based POST screen, which displays a number of PC diagnostic messages.
To exit the QuietBoot screen and run Setup, display the Multiboot menu, or simply display the PC diagnostic messages, you can simply press one of the hot keys described below.
The QuietBoot Screen stays up until just before the operating system loads unless:

- You press <ESC> to display the POST screen.
- You press <Del> to enter Setup.
- POST issues an error message.
- The BIOS or an option ROM requests keyboard input.

The following explains each of these situations.

5.1.3.2 Press <ESC>

1. Pressing <ESC> switches the POST screen and The boot process continues with the text-based POST screen until the end of POST, and then displays the BootFirst Menu, with these options:
1. Load the operating system from a boot device of your choice.
2. Enter Setup.
3. Exit the Boot First Menu (with <ESC>) and load the operating system from the boot devices in the order specified in Setup.

5.1.3.3 Press <Del>

Pressing < Del > at any time during POST enter Setup.

5.1.3.4 Keyboard Input Request

If the BIOS or an Option ROM (add-on card) requests keyboard input, QuietBoot switches over to the POST screen and the Option ROM displays prompts for entering the information. POST continues from there with the regular POST screen.

5.1.3.5 Phoenix Multiboot

Phoenix Multiboot expands your boot options by letting you choose your boot device, which could be a hard disk, floppy disk, CDROM, Flash Disk, SCSI or LAN. You can select your boot device in Setup, or you can choose a different device each time you boot during POST by selecting your boot device in **The Boot First Menu (ESC key)**.

Multiboot consists of:

The Setup Boot Menu

The Boot First Menu

5.2 Installing Drivers

5.2.1 Video Drivers

Various drivers are provided for different operating systems and software. To install a driver, refer to the Setup program located on the CD-ROM (provided with your board).

5.2.2 Ethernet Drivers

Various drivers are provided for different operating systems and software. To install a driver, use the Setup program and the ReadMe.bat file located on the CD-ROM (provided with your board).

5.2.3 Other Drivers

For other operating system drivers and installation instructions or for more information, visit our Web site at www.kontron.com or our FTP site at ftp.kontron.ca/support/ or you may also contact Kontron's Technical Support department.

5.3 Console Redirection (VT100 Mode)

The VT100 operating mode allows remote setups of the board. This configuration requires a remote terminal that must be connected to the board through a serial communication link.

5.3.1 Requirements

The terminal should emulate a VT100 or ANSI terminal. Terminal emulation programs such as Telix© or Procom© can also be used.

5.3.2 Setup & Configuration

Follow these steps to set up the VT100 mode:

1. Connect a monitor and a keyboard to your board and turn on the power.
2. Enter into the CMOS Setup program in the "Advanced" page, "Console Redirection" menu.
3. Select the VT100 mode and the appropriate COM port and save your setup.
4. Connect the communications cable.

Note:
If you do not require a full cable for your terminal, you can set up a partial cable by using only the TXD and RXD lines. To ignore control lines simply loop them back as shown in VT100 Partial Setup cable diagram.

5. Configure your terminal to communicate using the same parameters as in CMOS Setup.
6. Install the VT100 jumper. Reboot the board.
7. Use the remote keyboard and display to setup the BIOS.

Save the setup, exit, and disconnect the remote computer from the board to operate in stand-alone configuration.

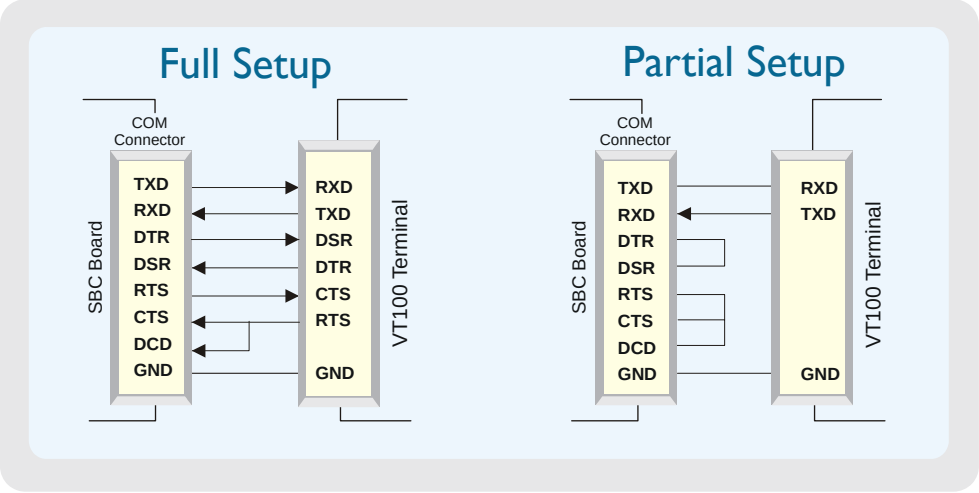
Console Redirection is done by refreshing the Video address @ B8000h at the selected BAUD rate. This means that a low baud rate refreshes the screen slowly, but the CPU time is maximized for the applications. A high BAUD rate refreshes the screen rapidly but the CPU is frequently interrupted by the Serial Port.

Console Redirection provided by Phoenix based BIOS offers various escape sequences to emulate keyboard function keys. The following table lists the escape sequences available.

Escape sequence	Function	Escape sequence	Function
Esc Del	Warm Reset	Esc [6 4 ~	(Ctrl-F1)
Esc O P	F1	Esc [6 5 ~	(Ctrl-F2)
Esc O Q	F2	Esc [6 6 ~	(Ctrl-F3)
Esc O R	F3	Esc [6 7 ~	(Ctrl-F4)
Esc O S	F4	Esc [6 8 ~	(Ctrl-F5)
Esc O w	F3	Esc [6 9 ~	(Ctrl-F6)
Esc O x	F4	Esc [7 0 ~	(Ctrl-F7)
Esc O t	F5	Esc [7 1 ~	(Ctrl-F8)
Esc O u	F6	Esc [7 2 ~	(Ctrl-F9)
Esc O q	F7	Esc [7 3 ~	(Ctrl-F10)
Esc O r	F8	Esc [7 4 ~	(Ctrl-F11)
Esc O p	F10	Esc [7 5 ~	(Ctrl-F12)

5.3.3 Running Without a Terminal

The board can boot up without a screen or terminal attached. If the speed is set to Auto and no terminal is connected, the speed is set to 115,200 bauds.
Furthermore, you can run without any console at all by simply not enabling VT100 Mode and by disabling the onboard video.

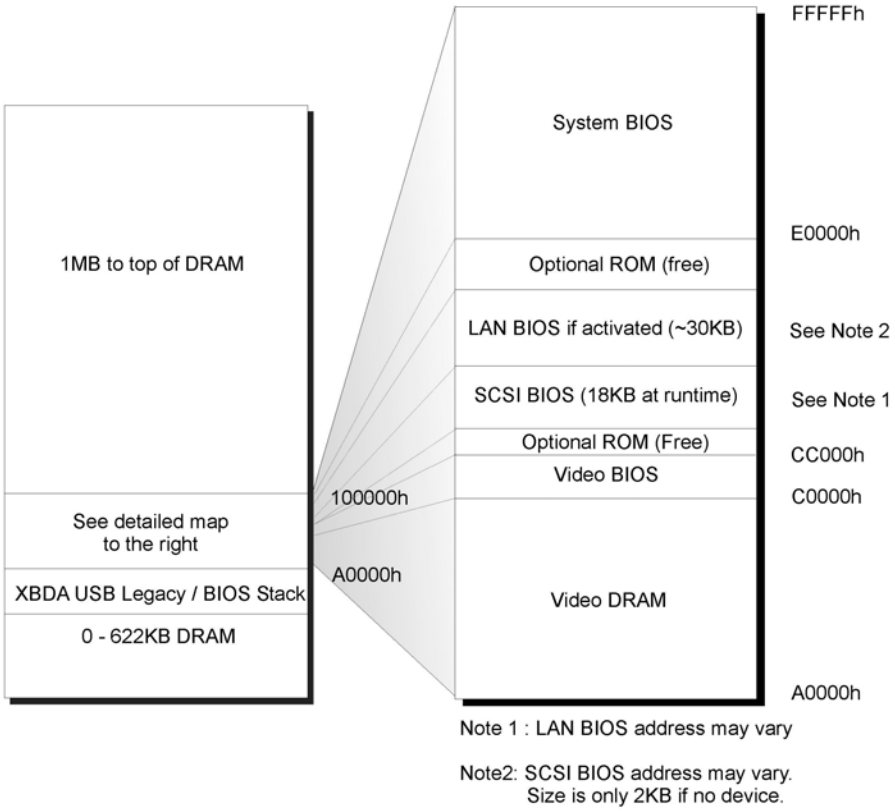


Appendix

Contents

A. Memory & I/O Maps

A.1 MEMORY MAPPING



Address	Function
00000-9B7FF	0-622 KB DRAM
9B800-9FFFF	622KB – 640 KB XBDA; USB Legacy / BIOS Stack
A0000-BFFFF	Video DRAM
C0000-CBFFF	Video BIOS
CC000-DBFFF	Optional ROM (Free) LAN BIOS around 30KB if activated, address may vary External SCSI BIOS 18KB-64KB , address may vary
E0000-FFFFF	System BIOS
100000-PCI Memory	DRAM available

A.2 I/O MAPPING

Address	Optional Address	Function
000-01F		DMA Controller 1
020-03F		Interrupt Controller 1
040-05F		Timer
060-06F		Keyboard
070-07F		Real-time clock
080-09F		DMA Page Register
0A0-0BF		Interrupt Controller 2
0C0-0DF		DMA Controller 2
0F0-0F1, 0F8-0FF		Math Coprocessor
190-1AB		Kontron Control Port
1F0-1F7, 3F6		Primary IDE
170-177, 376		Secondary IDE
3F0-3F7		Floppy Disk
3F8-3FF (COM1)	2F8-2FF (COM2)	Serial Port 1 (COM1 by default)
2F8-2FF (COM2)	3F8-3FF (COM1)	Serial Port 2 (COM2 by default)
400-0FFF		Chipset Reserved

B. Interrupt Lines

B.1 IRQ LINES

The board is fully PC compatible with interrupt steering for PCI plug and play compatibility.

Controller # 1		Controller # 2	
IRQ 0	Timer Output 0	IRQ 8	Real-Time Clock
IRQ 1	Keyboard (Output Buffer Full)	IRQ 9	Available [1]
IRQ 2	Cascade Controller # 2	IRQ 10	Available [1]
IRQ 3*	Serial Port 2	IRQ 11	Available [1]
IRQ 4*	Serial Port 1	IRQ 12	PS/2 Mouse
IRQ 5*	BMC_INT/Available [1]	IRQ 13	Coprocessor Error
IRQ 6*	Floppy Controller	IRQ 14	Primary IDE * or available [1]
IRQ 7*	BMC_INT/Available [1]	IRQ 15	Secondary IDE * or available [1]

* :All functions marked with an asterisk (*) can be disabled or reconfigured.
1 Available lines service on board and external PCI devices in Legacy mode (Boot interrupt).

B.2 PCI INTERRUPTS

Interrupt ICH3	
IRQ14	IDE 0
IRQ15	IDE 1
PIRQA#	P62H2 (Boot interrupt)
PIRQB#	MOBILITY-M
PIRQC#	LAN 10/100 Ethernet Management
PIRQD#	USB
PIRQE#	BMC_SMI
PIRQF#	FPGA_INT
PIRQH#	FPGA_NMI

Interrupt P64H2	
PCI BUS A	
INT 0	PMC A INT A
INT 1	PMC A INT B
INT 2	PMC A INT C
INT 3	PMC A INT D
PCI BUS B	
INT 0	PMC B INT A
INT 1	PMC B INT B
INT 2	PMC B INT C
INT 3	PMC B INT D
INT 4	GLAN 2
INT 5	GLAN 1
INT 6	CPCI INT A
INT 7	CPCI INT B
INT 8	CPCI INT C
INT 9	CPCI INT D
INT 10	CPCI MEZZ. INT A*
INT 11	CPCI MEZZ. INT B*
INT 12	CPCI MEZZ. INT C*
INT 13	CPCI MEZZ. INT D*
INT 14	BRDG. MEZZ INT*

* On request only (SMR) 8HP option mezzanine.

C. Kontron Extension Registers

C.1 FPGA/CPLD REGISTERS DEFINITION

Unused (shaded) bits are reserved. It is strongly recommended not to modify unused bit to insure compatibility with other product. Base addresses are fixed. It can be changed but no option will be supported in the BIOS setup. We strongly recommend using the default base address. Bits marked NU are not used on this board. Writing to such bit does nothing and reading is undefined, either 0 or 1 may be returned. Next table present I/O addressee for each register

Legend:

Symbol		Signification
U	=	Unchanged (stay unchanged after reset)
X	=	Not Defined (bit not used on this board)
NU	=	Not Used

C.2 OVERVIEW

FPGA/CPLD registers

	Address	D7	D6	D5	D4	D3	D2	D1	D0
READ	0x190	*NU*	*NU*	*NU*	RS485	RS232	ST1	*NU*	*NU*
WRITE	0x190	*NU*	*NU*	*NU*	RS485	RS232	ST1	*NU*	*NU*
READ	0x191	*NU*	*NU*	WD0	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x191	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x192	BL_ST	BL_EN	SW_O	*NU*	*NU*	LOCK	*NU*	*NU*
WRITE	0x192	BL_ST	BL_EN	*NU*	*NU*	*NU*	LOCK	*NU*	*NU*
READ	0x193	*NU*	*NU*	*NU*	*NU*	IDCHIP	*NU*	*NU*	*NU*
WRITE	0x193	*NU*	*NU*	*NU*	*NU*	IDCHIP	*NU*	*NU*	*NU*
READ	0x194	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x194	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x195	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x195	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x196	WDEN	WDD2	WDD1	WDD0	*NU*	*NU*	*NU*	*NU*
WRITE	0x196	WDEN	WDD2	WDD1	WDD0	*NU*	*NU*	*NU*	*NU*
READ	0x197	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x197	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x198	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x198	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x199	VGA_EN#	VT100#	BSPD	BSPD	BSPD	*NU*	*NU*	EN_LAN
WRITE	0x199	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	EN_LAN
READ	0x19A	LB_S1	LB_S0	LB_G	LB_R	LA_S1	LA_S0	LA_G	LA_R
WRITE	0x19A	LB_S1	LB_S0	LB_G	LB_R	LA_S1	LS_S0	LA_G	LA_R
READ	0x19B	ST2	ST1	ST0	GA4	GA3	GA2	GA1	GA0
WRITE	0x19B	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x19C	TEST	FWH_LOCK	*NU*	P_COM2	BMC_2EXT	BMC_COM	BMC_RST	BMC_PRG
WRITE	0x19C	NU	*NU*	*NU*	P_COM2	*NU*	BMC_COM	BMC_RST	BMC_PRG
READ	0x19D	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x19D	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x19E	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x19E	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x19F	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x19F	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x1A0	*NU*	*NU*	*NU*	*NU*	*NU*	SW_EN	WD_EN	ENUM_EN
WRITE	0x1A0	*NU*	*NU*	*NU*	*NU*	*NU*	SW_EN	WD_EN	ENUM_EN
READ	0x1A1	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x1A1	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x1A2	*NU*	*NU*	*NU*	*NU*	*NU*	SWITCH	WDOG	ENUM
WRITE	0x1A2	*NU*	*NU*	*NU*	*NU*	*NU*	SWITCH	WDOG	*NU*
READ	0x1A3	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
WRITE	0x1A3	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
READ	0x1A4	*NU*	*NU*	*NU*	*NU*	*NU*	TBL	WP	MEZZ
WRITE	0x1A4	*NU*	*NU*	*NU*	*NU*	*NU*	TBL	WP	*NU*

C.3 0190H: COM2 RS232/422/485 BUFFER CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x190	READ	*NU*	*NU*	*NU*	RS485	RS232	ST1	*NU*	*NU*
	WRITE	*NU*	*NU*	*NU*	RS485	RS232	ST1	*NU*	*NU*
	Reset	*X*	*X*	*X*	0	1	0	*X*	*X*

RS485	RS232	ST1	Description
0	1	X	RS232 mode (default)
1	0	0	RS485/422 point-to-point mode: - RX is always enable. - TX enabled when COM2 RTS is asserted.
1	0	1	RS485 party line mode: - RX enabled when COM2 RTS is deasserted. - TX enabled when COM2 RTS is asserted.
1	1	X	Illegal. This puts the buffers in RS232 mode.
0	0	X	Illegal. This puts the buffers in RS232 mode. This is the condition on power up. Value is changed by the BIOS.

C.4 0191H: RESET HISTORY

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x193	READ	*NU*	*NU*	WDO	*NU*	*NU*	*NU*	*NU*	*NU*
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
	Reset	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

WDO Board reseted by the watchdog

C.5 0192H: BRACKET SWITCH, BLUE LED

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x192	READ	BL_ST	BL_EN	SW_O	*NU*	*NU*	LOCK	*NU*	*NU*
	WRITE	BL_ST	BL_EN	*NU*	*NU*	*NU*	LOCK	*NU*	*NU*
	Reset	0	0	*X*	*X*	*X*	1	*X*	*X*

BL_ST Blue LED state.
BL_EN Blue LED control enable
SW_O When "1", the bracket switch is open.
LOCK When "1", the enable bit of the watchdog (WDEN) can't be modified.

C.6 0193H: ID CHIP

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x193	READ	*NU*	*NU*	*NU*	*NU*	IDCHIP	*NU*	*NU*	*NU*
	WRITE	*NU*	*NU*	*NU*	*NU*	IDCHIP	*NU*	*NU*	*NU*
	Reset	*X*	*X*	*X*	*X*	Z	*X*	*X*	*X*

IDCHIP ID Chip (serial number) control. Open-drain output with pin readback.

C.7 0196H: WATCHDOG CONTROL

This is a "Kontron SBC" standard dual stage watchdog. However, the second stage time increases from 1ms to 16ms to ease the interrupt handling when using ISA interrupt. So, either a NMI or a legacy interrupt will generate after the specified timeout. Then, the watchdog must be triggered either by writing the WDD[2:0] bits or by clearing the interrupt bit in the 1A2h register. Failure to trigger the watchdog within 16ms will reset the system. If interrupts are disabled, the watchdog reverts to a single stage one.

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x196	READ	WDEN	WDD2	WDD1	WDD0	*NU*	*NU*	*NU*	*NU*
	WRITE	WDEN	WDD2	WDD1	WDD0	*NU*	*NU*	*NU*	*NU*
	Reset	0	1	1	1	*X*	*X*	*X*	*X*

WDEN — Enable. Lockable with bit LOCK.
WDD[2..0] — Timeout selection. A write to this register triggers the watchdog. Timeout as follow:
000: 0.016s
001: 0.065s
010: 0.262s
011: 1.048s
100: 4.194s
101: 16.78s
110: 67.11s
111: 268.4s

C.8 0197H: NMI CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x197	READ	*NU*	*NU*	*NU*	*NU*	SWNMIEN	SWNMIEN	WDNMIEN	WDNMI
	WRITE	*NU*	*NU*	*NU*	*NU*	SWNMIEN	*NU*	WDNMIEN	*NU*
	Reset	*X*	*X*	*X*	*X*	0	*X*	0	*X*

WDNMI — Watchdog NMI occur when 1
WDNMIEN — Enable NMI on watchdog timer when 1
SWNMI — Front Panel Switch NMI occur when 1
SWNMIEN — Enable NMI on CPCI SWITCH when 1

C.9 0199H: PCI DEVICE ENABLE & JUMPER CONFIGURATION

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x197	READ	VGA_EN	VT100#	BSPD	BSPD	BSPD	*NU*	*NU*	*NU*
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
	Reset	*X*	*X*	*X*	*X*	*X*	*X*	*X*	*X*

VGA_EN — Read jumper for VGA enable
VT100# — Read jumper for VT100
BSPD — CPCI Maximal speed

C.10 019AH: USER LED CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x19C	READ	LB_S1	LB_S0	LB_G	LB_R	LA_S1	LA_S0	LA_G	LA_R
	WRITE	LB_S1	LB_S0	LB_G	LB_R	LA_S1	LS_S0	LA_G	LA_R
	Reset	0	0	0	0	1	1	0	0

LA_R Control red component of user led 'A' Led is on when this bit is set to '1'
LA_G Control green component of user led 'A'. Led is on when this bit is set to '1'
SA_S[0:1] Mode selection for user led 'A"
LB_R Control red component of user led 'B'. Led is on when this bit is set to '1'
LB_G Control green component of user led 'B'. Led is on when this bit is set to '1'
SB_S[0:1] Mode selection for user led 'B"
S[0:1] Led Mode
00: IDE activity
01: BMC debug LED
10: Post Code debug LED
11: User control

C.11 019BH: BACKPLANE INFORMATION

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
019Bh	READ	ST2	ST1	ST0	GA4	GA3	GA2	GA1	GA0
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*	*NU*
	Reset	State of hardware pins							

GA[4..0] Geographical address.
ST[2..0] Segment type (As defined in PICMG2.0R3.0 ECR#2).
000: Nominal left
001: Nominal right
111: Backplane do not provide segment type
other: reserved

C.12 019CH: BMC CONTROL

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x19C	READ	TEST	*NU*	BMC_LOCK	P_COM2	BMC_2EXT	BMC_COM	BMC_RST	BMC_PRG
	WRITE	*NU*	*NU*	BMC_LOCK	P_COM2	*NU*	BMC_COM	BMC_RST	BMC_PRG
	Reset	*X*	1	1	0	*X*	0	0	0

TEST If set, the SBC is inserted in a CPCI test backplane. This is used for Kontron test platform. Not used by SMB
BMC_2EXT When '1' The BMC com port is routed to COM2 buffer
BMC_COM When '1', the SIO is connected to BMC. When '0', the SIO is connected to output buffer. This bit is ignored if BMC_TAKE_COM = '1'.
BMC_RST When '1', reset BMC
BMC_PRG When '1', set BMC in program mode. COM2 is redirected to BMC to allow bootstrapping the microcontroller.
BMC_LOCK When TEST# is '1' BMC_LOCK has no effect on BMC_RST bit. When TEST# is '0' and BMC_LOCK is '0' BMC_RST bit is in normal operation. When TEST# is '0' and BMC_LOCK is '1', BMC is in Reset
P_COM2 Redirected postcode on serial port when is set to 1

Signal routing follow this table:

BMC_PRG	TAKE_COM2_N	BMC_COM	Routing
0	1	0	SIO to buffers (default), BMC RXD = 1
0	1	1	SIO to BMC, Buffers TXD = 1
0	0	X	BMC to buffer, Host RXD = 1
1	X	X	SIO to BMC, Buffers TXD = 1

C.13 01A0H: PCI INTERRUPT ENABLE

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A0	READ	0	0	0	0	ISA3	ISA2	ISA1	ISA1
	WRITE	0	0	0	0	ISA3	ISA2	ISA1	ISA1
	Reset	0	0	0	0	0	0	0	0

ISA[3..0] ISA IRQ number

C.14 01A1H: INTERRUPT ENABLE

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A0	READ	*NU*	*NU*	*NU*	*NU*	*NU*	SW_EN	WD_EN	ENUM_EN
	WRITE	*NU*	*NU*	*NU*	*NU*	*NU*	SW_EN	WD_EN	ENUM_EN
	Reset	*X*	*X*	*X*	*X*	*X*	0	0	0

SW_EN Set this bit to enable interrupt on switch event.
WD_EN Enable watchdog interrupt
ENUM_EN Enable ENUM interrupt. The interrupt is generated for both onboard CPCI interface and the mezzanine CPCI interface. On this SBC, the PLX6540 PCIX-PCIX bridge can handle the ENUM event as an alternate way.

C.15 01A2H: INTERRUPT STATUS

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A2	READ	RSV	RSV	*NU*	*NU*	*NU*	SWITCH	WDOG	ENUM
	WRITE	RSV	RSV	*NU*	*NU*	*NU*	SWITCH	WDOG	*NU*
	Reset	*X*	*X*	*X*	*X*	*X*	0	0	0

SWITCH A one indicates a switch event has occurred. Switch state can be read on 0191h bit 5. Write a one to this bit clears the interrupt.
WDOG A one indicates a watchdog interrupt has occurred. Writing a one to this bit clears the watchdog and clears the interrupt. Reset will occur 16ms after the interrupt.
ENUM A one indicates an ENUM has occurred on either the onboard CPCI interface or the mezzanine interface. Writing a one to this register does nothing. The interrupt condition must be cleared in the source PCI device.
RSV Rewrite what is read.

C.16 01A4H: CONTROL FWH BOOT BLOCK AND MEZZANINE

Address	Action	D7	D6	D5	D4	D3	D2	D1	D0
0x1A3	READ	*NU*	*NU*	FWH_MEZZ_BIT	*NU*	*NU*	TBL	WP	MEZZ
	WRITE	*NU*	*NU*	FWH_MEZZ_BIT	*NU*	*NU*	TBL	WP	*NU*
	Reset	*X*	*X*	MEZZ	*X*	*X*	0	1	*X*

FWH_MEZZ_BIT	Select FWH Mezzanine BIOS. When this bit is '0' net fwh_mezz is sink to GND and onboard FWH have address 0. When this bit is '1', PLD float this net and onboard FWH have address 1. This bit has no effect when we don't have FWH Mezzanine.
TBL	TOP SECTOR LOCK: When low, prevents programming or sector erase to the highest addressable sector (7 in a 4-Mbit, 15 in an 8-Mbit component) regardless of the state of the lock registers TBL high disables hardware write protection for the top sector, though register-based protection still applies. The status of TBL does not affect the status of sector-locking registers. When we lock register with fwh_lock (Reg_BMCCTR) TBL state comes automatically at '0'
WP	WRITE-PROTECT: When low, prevents programming or sector erase to all but the highest addressable sectors (0 - 6 in a 4-Mbit, 0 - 14 in an 8-Mbit component), regardless of the state of the corresponding lock registers. WP-high disables hardware write protection for these sectors, though register-based protection still applies. The status of TBL does not affect the status of sector-locking registers.When we lock register with fwh_lock (Reg_BMCCTR) TBL state comes automatically at '0'
MEZZ	Emergency Bios mezz is preset when this bit is set to '1'

D. Connector Pinouts

D.1 CONNECTORS AND HEADERS SUMMARY

Connector	Description
J1	CPCI Bus connector
J2	CPCI Bus connector
J3	CPCI I/O connector
J4	CPCI I/O connector
J5	CPCI I/O connector
J6	POST Code
J7, J8	Memory SODIMM 1-2
J9	Ethernet Management
J10	COM1 (Faceplate) (RJ-45)
J11	USB (Faceplate)
J12	Compact Flash
J13	Hot Swap Switch
J14	IDE Mezzanine
J16	JTAG
JN1A-JN4A	64-bit PCIX Mezzanine & PIM
JN1B-JN3B	64-bit PCIX Mezzanine
SW1	Reset Button (faceplate)
BT1	Battery
LP1	LEDs

D.2 CPCI BUS (J1)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	VCCE	-12VE	RSV	+12VE	VCCE
2	RSV	VCCE	RSV	RSV	RSV
3	INTA#	INTB#	INTC#	VCCE	INTD#
4	IPMB_PWR	HEALTHY#	VI/O	INTP	INTS
5	RSV	RSV	RST#	GND	GNT0#
6	REQ0#	PCI_PRESENT#	VCC3E	CLK0	AD31
7	AD30	AD29	AD28	GND	AD27
8	AD26	GND	VI/O	AD25	AD24
9	CBE3#	IDSEL	AD23	GND	AD22
10	AD21	GND	VCC3E	AD20	AD19
11	AD18	AD17	AD16	GND	CBE2#
12					
13			**KEY AREA**		
14					
15	VCC3E	FRAME#	IRDY#	BD_SEL#	TRDY#
16	DEVSEL#	PCIXCAP	VI/O	STOP#	LOCK#
17	VCC3E	IPMB0_SCL	IPMB0_SDA	GND	PERR#
18	SERR#	GND	VCC3E	PAR	CBE1#
19	VCC3E	AD15	AD14	GND	AD13
20	AD12	GND	VI/O	AD11	AD10
21	VCC3E	AD9	AD8	M66EN	CBE0#
22	AD7	GND	VCC3E	AD6	AD5
23	VCC3E	AD4	AD3	VCCE	AD2
24	AD1	VCCE	VI/O	AD0	ACK64#
25	VCCE	REQ64#	ENUM#	VCC3E	VCCE

Active Low

Long pins : 3D, 4C,5D, 6C, 7D, 9D, 10D, 17D, 19D, 22C, 23D, 24C

Short pins : 9B, 15D

D.3 CPCI BUS (J2)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	S_CLK1	GND	REQ1#	GNT1#	REQ2#
2	S_CLK2	S_CLK3	SYSEN#	GNT2#	REQ3#
3	S_CLK4	GND	GNT3#	REQ4#	GNT4#
4	VI/O	RSV	CBE7#	GND	CBE6#
5	CBE5#	64_EN#	VI/O	CBE4#	PAR64
6	AD63	AD62	AD61	GND	AD60
7	AD59	GND	VI/O	AD58	AD57
8	AD56	AD55	AD54	GND	AD53
9	AD52	GND	VI/O	AD51	AD50
10	AD49	AD48	AD47	GND	AD46
11	AD45	GND	VI/O	AD44	AD43
12	AD42	AD41	AD40	GND	AD39
13	AD38	GND	VI/O	AD37	AD36
14	AD35	AD34	AD33	GND	AD32
15	RSV	GND	FAL#	REQ5#	GNT5#
16	RSV	RSV	DEG#	GND	RSV
17	RSV	GND	PRST#	REQ6#	GNT6#
18	RSV	RSV	RSV	GND	RSV
19	GND	GND	IMPB1_SDA	SMB1_SCL	SMB_ALERT#
20	CLK5	GND	RSV	GND	RSV
21	CLK6	GND	RSV	RSV	RSV
22	GA4	GA3	GA2	GA1	GA0

Active Low

D.4 CPCI I/O (J3)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	COM1:RTS	COM1:RXD	COM1:DSR	COM1:DCD	ID1
2	COM1:RI	COM1:DTR	COM1:CTS	COM1:TXD	MOUSE:CLK
3	COM2:RTS	COM2:RXD	COM2:DSR	COM2:DCD	MOUSE:DATA
4	COM2:RI	COM2:DTR	COM2:CTS	COM2:TXD	KB:DATA
5	VGA:BLUE	VGA:HSYNC	VGA:VSYNC	VGA:SCL	KB:CLK
6	VGA:RED	VGA:GREEN	VGA:SDA	POST:CLK	POST:DATA
7	VCC3	ID2	ID3	ID4	SPEAKER
8	USB0:DATA-	USB0:DATA+	GND	RSV	RSV
9	USB1:DATA-	USB1:DATA+	GND	RSV	RSV
10	USB1:VCC	USB0:VCC	GND	RSV	RSV
11	LAN3:ERX+	LAN3:ERX-	GND	RSV	RSV
12	LAN3:ETX+	LAN3:ETX-	GND	RSV	RSV
13	LAN2:ACT	LAN1:ACT	RSV	LAN3:ACT	RSV
14	LAN2:LINK	LAN1:LINK	LAN:CT	LAN3:LINK#	RSV
15	LAN1:DB+	LAN1:DB-	GND	LAN1:DD+	LAN1:DD-
16	LAN1:DA+	LAN1:DA-	GND	LAN1:DC+	LAN1:DC-
17	LAN2:DB+	LAN2:DB-	GND	LAN2:DD+	LAN2:DD-
18	LAN2:DA+	LAN2:DA-	GND	LAN2:DC+	LAN2:DC-
19	VCC	VCC	VCC3	+12V	-12V

D.5 CPCI I/O (PIM) (J4)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	PIM:61	PIM:63	GND	PIM:62	PIM:64
2	PIM:57	PIM:59	GND	PIM:58	PIM:60
3	GND	GND	GND	GND	GND
4	PIM:53	PIM:55	GND	PIM:54	PIM:56
5	PIM:49	PIM:51	GND	PIM:50	PIM:52
6	GND	GND	GND	GND	GND
7	PIM:45	PIM:47	GND	PIM:46	PIM:48
8	PIM:41	PIM:43	GND	PIM:42	PIM:44
9	GND	GND	GND	GND	GND
10	PIM:37	PIM:39	GND	PIM:38	PIM:40
11	PIM:33	PIM:35	GND	PIM:34	PIM:36
12					
13			**KEY AREA**		
14					
15	PIM:29	PIM:31	GND	PIM:30	PIM:32
16	PIM:25	PIM:27	GND	PIM:26	PIM:28
17	GND	GND	GND	GND	GND
18	PIM:21	PIM:23	GND	PIM:22	PIM:24
19	PIM:17	PIM:19	GND	PIM:18	PIM:20
20	GND	GND	GND	GND	GND
21	PIM:13	PIM:15	GND	PIM:14	PIM:16
22	PIM:9	PIM:11	GND	PIM:10	PIM:12
23	RSV	VCC	GND	RSV	VCC3
24	PIM:5	PIM:7	GND	PIM:6	PIM:8
25	PIM:1	PIM:3	GND	PIM:2	PIM:4

D.6 CPCI I/O (SCSI) (J4)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	D12+	D12-	GND	D13+	D13-
2	D14+	D14-	GND	D15+	D15-
3	GND	GND	GND	GND	GND
4	DP1+	DP1-	GND	D0+	D0-
5	D1+	D1-	GND	D2+	D2-
6	GND	GND	GND	GND	GND
7	D3+	D3-	GND	D4+	D4-
8	D5+	D5-	GND	D6+	D6-
9	GND	GND	GND	GND	GND
10	D7+	D7-	GND	DP0+	DP0-
11	DIFFSENS	TERMPW	GND	TERMPW	TERMPW
12					
13			KEY AREA		
14					
15	TERMPW	TERMPW	GND	TERMPW	TERMPW
16	TERMPW	TERMPW	GND	ATN+	ATN-
17	GND	GND	GND	GND	GND
18	BSY+	BSY-	GND	ACK+	ACK-
19	RST+	RST-	GND	MSG+	MSG-
20	GND	GND	GND	GND	GND
21	SEL+	SEL-	GND	CD+	CD-
22	REQ+	REQ-	GND	IO+	IO-
23	N.C.	VCC	GND	N.C.	VCC3
24	D8+	D8-	GND	D9+	D9-
25	D10+	D10-	GND	D11+	D11-

D.7 CPCI I/O (J5)

Pin	ROW A	ROW B	ROW C	ROW D	ROW E
1	GND	GND	GND	GND	GND
2	RSV	RSV	GND	RSV	RSV
3	GND	GND	GND	GND	GND
4	RSV	RSV	GND	RSV	RSV
5	GND	GND	GND	GND	GND
6	RSV	RSV	GND	RSV	RSV
7	GND	GND	GND	GND	GND
8	RSV	RSV	GND	RSV	RSV
9	GND	GND	GND	GND	GND
10	FD:MSEN0	FD:MSEN1	GND	RSV	RSV
11	FD:MTR0#	FD:INDEX#	GND	FD:FDEDIN#	FD:DENSEL#
12	FD: DIR#	FD: MTR1#	GND	FD: DSEL0#	FDE: DSEL1#
13	FD: TRK0#	FD: WGATE#	GND	FD: WDATA#	FD: STEP#
14	FD: DSKCHG#	FD: HDSEL#	GND	FD: RDATA#	FD: WRPROT#
15	IDE1:D6	IDE1:D8	GND	IDE1:D7	IDE1:RESET#
16	IDE1:D4	IDE1:D10	GND	IDE1:D5	IDE1:D9
17	IDE1:D2	IDE1:D12	GND	IDE1:D3	IDE1:D11
18	IDE1:D0	IDE1:D14	GND	IDE1:D1	IDE1:D13
19	IDE1:IOR#	IDE1:IOW#	GND	IDE1:REQ	IDE1:D15
20	RSV	IDE1:IRQ	GND	IDE1: ACK#	IDE1:IORDY
21	IDE1:A2	IDE1:A0	GND	IDE1:A1	IDE1:PDIAG#
22	IDE1:ACT#	IDE1:CS3#	GND	IDE1:CS0#	BATT

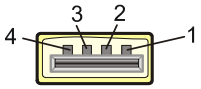
Active Low

D.8 SERIAL PORT 1 - RS-232 (J10)

Signal	Pin		Pin	Signal
RTS	1		5	GND
DTR	2		6	RXD
TXD	3		7	DSR
GND	4		8	CTS

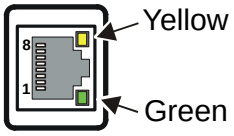
D.9 USB (LOCATED ON FACEPLATE) (J11)

Signal	Pin
VCC	1
DATA-	2
DATA+	3
GND	4



D.10 ETHERNET MANAGEMENT (J9)

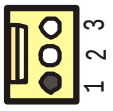
Signal	
TX+	1
TX-	2
RX+	3
nu	4
nu	5
RX-	6
nu	7
nu	8



Note
These two LEDs might be reversed.

D.11 HOT SWAP SWITCH (J13)

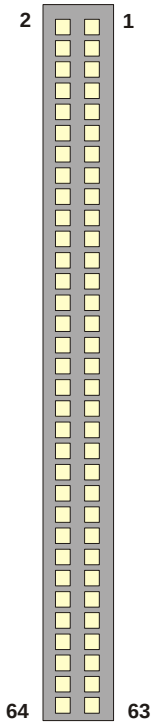
Signal	Pin
VCC3E	1
SW_OPEN#	2
SW_CLOSE#	3



Active Low Signal

D.12 IDE MEZZANINE (J14)

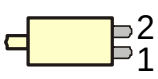
Signal	Pin		Pin	Signal
P64GNT#_MEZ2	1		2	IPMB0_SDA
GND	3		4	IPMB0_SCL
CLK66_MEZ	5		6	GND
VCC	7		8	CLK66_PMC_8HP
P64REQ#_MEZ	9		10	GND
P64GNT#_MEZ	11		12	INTB_P64MEZZ#
INT_BRDG_MEZ	13		14	INTA_P64MEZZ#
INTD_P64MEZZ#	15		16	MEZZ_ENUM#
INTC_P64MEZZ#	17		18	IDE0:MS#/SLV
P64REQ#_MEZ2	19		20	IDE0:ACT#
IDE0:CS1#	21		22	GND
IDE0:DA2	23		24	IDE0:CS0#
GND	25		26	IDE0:DA0
IDE0:PDIAG#	27		28	GND
IDE0:DA1	29		30	IDE0:IRQ
GND	31		32	IDE0:DMACK#
IDE0:IORDY	33		34	GND
IDE0:IOR#	35		36	IDE0:IOW#
BD_SEL_MEZZ#	37		38	IDE0:DMARQ
IDE0:D0	39		40	HEALTHY#_BP
IDE0:D1	41		42	IDE0:D15
RSV	43		44	IDE0:D14
IDE0:D2	45		46	RSV
IDE0:D3	47		48	IDE0:D13
RSV	49		50	IDE0:D12
IDE0:D4	51		52	RSV
IDE0:D5	53		54	IDE0:D11
RSV	55		56	IDE0:D10
IDE0:D6	57		58	RSV
IDE0:D7	59		60	IDE0:D9
RSV	61		62	IDE0:D8
IDE:RESET#	63		64	RSV



Active Low

D.13 RESET SWITCH (SW1)

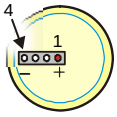
Signal	Pin
GND	1
RESET#	2



Active Low Signal

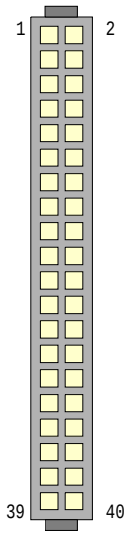
D.14 CMOS BATTERY BACKUP CONNECTOR (BT1)

Signal	Pin
Battery (+)	1
Battery (-)	4



D.15 COMPACTFLASH™ (J12)

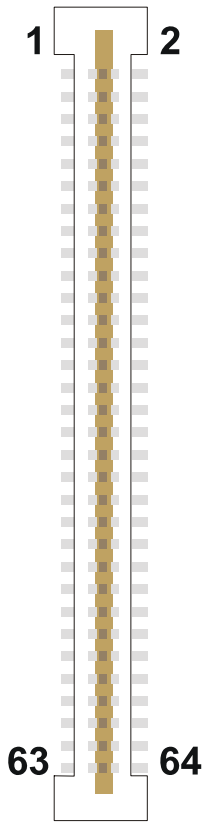
Signal	Pin		Pin	Signal
D11	1		2	GND
D12	3		4	D3
D13	5		6	D4
D14	7		8	D5
D15	9		10	D6
CS1#	11		12	D7
DMACK#	13		14	CS0#
DMARQ	15		16	IOR#
PDIAG#	17		18	IOW#
IRQ15	19		20	VCC
VCC	21		22	VCC
GND	23		24	GND
RESET#	25		26	GND
CSEL	27		28	A2
A1	29		30	DASP#
A0	31		32	IORDY
D0	33		34	D8
D1	35		36	D9
D2	37		38	D10
IOCS16#	39		40	GND



Active Low Signal

D.16 JNA1 & JNB1– PMC (JNA1 & JNB1)

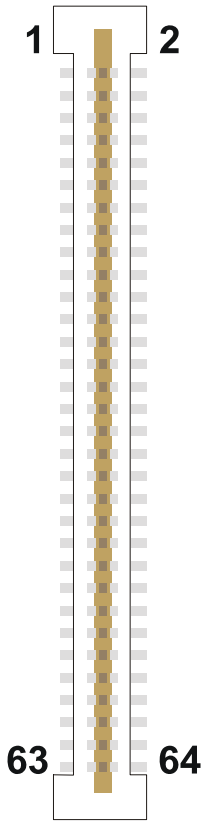
Signal	Pin		Pin	Signal
N.C.	1		2	-12V
GND	3		4	INTA_P64PMC#
INTB_P64PMC#	5		6	INTC_P64PMC#
BUSMODE1#	7		8	VCC
INTD_P64PMC#	9		10	N.C.
GND	11		12	VCC3E
CLK66_PMC	13		14	GND
GND	15		16	P64GNT#_PMC
P64REQ#_PMC	17		18	VCC
VIO	19		20	P64AD31
P64AD28	21		22	P64AD27
P64AD25	23		24	GND
GND	25		26	P64C/BE#3
P64AD22	27		28	P64AD21
P64AD19	29		30	VCC
VIO	31		32	P64AD17
P64FRAME#	33		34	GND
GND	35		36	P64IRDY#
P64DEVSEL#	37		38	VCC
PCIXCAP/GND	39		40	P64LOCK#
RSV	41		42	SBO#
P64PAR	43		44	GND
VIO	45		46	P64AD15
P64AD12	47		48	P64AD11
AD9	49		50	VCC
GND	51		52	P64C/CBEO#
P64AD6	53		54	P64AD5
P64AD4	55		56	GND
VIO	57		58	P64AD3
P64AD2	59		60	P64AD1
P64AD0	61		62	VCC
GND	63		64	P64REQ64#



Active Low

D.17 JNA2 & JNB2– PMC (JNA2 & JNB2)

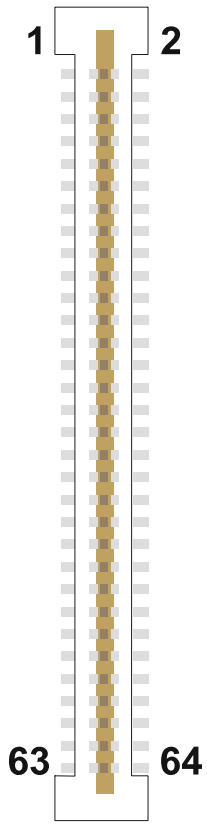
Signal	Pin		Pin	Signal
+12V	1		2	RSV
RSV	3		4	N.C.
RSV	5		6	GND
GND	7		8	N.C.
N.C.	9		10	N.C.
BMODE2#	11		12	VCC3
PCIRST#	13		14	BMODE3#
VCC3	15		16	BMODE4#
N.C.	17		18	GND
P64AD30	19		20	P64AD29
GND	21		22	P64AD26
P64AD24	23		24	VCC3
IDSEL_PMC	25		26	P64AD23
VCC3	27		28	P64AD20
P64AD18	29		30	GND
P64AD16	31		32	P64C/BE2#
GND	33		34	N.C.
P64TRDY#	35		36	VCC3
GND	37		38	P64STOP#
P64PERR#	39		40	GND
VCC3	41		42	P64SERR#
P64C/BE1#	43		44	GND
P64AD14	45		46	P64AD13
P64M66EN	47		48	P64AD10
P64AD8	49		50	VCC3
P64AD7	51		52	N.C.
VCC3	53		54	N.C.
N.C.	55		56	GND
N.C.	57		58	N.C.
GND	59		60	N.C.
P64ACK64#	61		62	VCC3
GND	63		64	N.C.



Active Low

D.18 JNA3 & JNB3– PMC (JNA3 & JNB3)

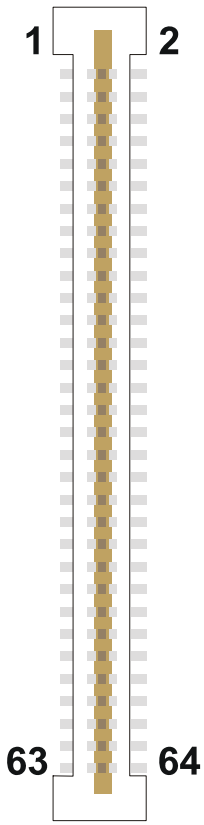
Signal	Pin		Pin	Signal
N.C.	1		2	GND
GND	3		4	P64C/BE7#
P64C/BE6#	5		6	P64C/BE5#
P64C/BE4#	7		8	GND
VIO	9		10	P64PAR64
P64AD63	11		12	P64AD62
P64AD61	13		14	GND
GND	15		16	P64AD60
P64AD59	17		18	P64AD58
P64AD57	19		20	GND
VIO	21		22	P64AD56
P64AD55	23		24	P64AD54
P64AD53	25		26	GND
GND	27		28	P64AD52
P64AD51	29		30	P64AD50
P64AD49	31		32	GND
GND	33		34	P64AD48
P64AD47	35		36	P64AD46
P64AD45	37		38	GND
VCC3	39		40	P64AD44
P64AD43	41		42	P64AD42
P64AD41	43		44	GND
GND	45		46	P64AD40
P64AD39	47		48	P64AD38
P64AD37	49		50	GND
GND	51		52	P64AD36
P64AD35	53		54	P64AD34
P64AD33	55		56	GND
VIO	57		58	P64AD32
N.C.	59		60	N.C.
N.C.	61		62	GND
GND	63		64	N.C.



Active Low

D.19 JN4A – PIM (JN4A)

Signal	Pin		Pin	Signal
P1+	1		2	P2+
P1-	3		4	P2-
P3+	5		6	P4+
P3-	7		8	P4-
P5+	9		10	P6+
P5-	11		12	P6-
P7+	13		14	P8+
P7-	15		16	P8-
P9+	17		18	P10+
P9-	19		20	P10-
P11+	21		22	P12+
P11-	23		24	P12-
P13+	25		26	P14+
P13-	27		28	P14-
P15+	29		30	P16+
P15-	31		32	P16-
P17+	33		34	P18+
P17-	35		36	P18-
P19+	37		38	P20+
P19-	39		40	P20-
P21+	41		42	P22+
P21-	43		44	P22-
P23+	45		46	P24+
P23-	47		48	P24-
P25+	49		50	P26+
P25-	51		52	P26-
P27+	53		54	P28+
P27-	55		56	P28-
P29+	57		58	P30+
P29-	59		60	P30-
P31+	61		62	P32+
P31-	63		64	P32-



Active Low

E. BIOS Setup Error Codes

E.1 POST BEEP

Recoverable POST Errors

Whenever a recoverable error occurs during POST, *Phoenix* BIOS displays an error message describing the problem.

Phoenix BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (no card installed or faulty) or if an external ROM module does not properly checksum to zero.

An external ROM module (e. g. VGA) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.

E.1.1 Terminal POST Errors

There are several POST routines that issue a **POST Terminal Error** and shut down the system if they fail. Before shutting down the system, the terminal error handler issues a beep code signifying the test point error, writes the error to port 80h, attempts to initialize the video, and writes the error in the upper left corner of the screen (using both mono and color adapters).

The routine drives the beep code from the test point error as follows:

1. The 8- bit error code is broken down to four 2 bit groups (Discard the most significant group if it is 00).
2. Each group is made one- based (1 through 4) by adding 1.
3. Short beeps are generated for the number in each group.

Example:
Test point 01Ah = 00 01 10 10 = 1- 2- 3- 3 beeps

Test Points and Beep Codes

At the beginning of each POST routine, the BIOS outputs the test point error code to I/O address 80h. Use this code during troubleshooting to establish at what point the system failed and what routine was being performed.

If the BIOS detects a terminal error condition, it halts POST after issuing a terminal error beep code (See above) and attempts to display the error code on upper left corner of the screen and on the port 80h LED display.

If the system hangs before the BIOS can process the error, the value displayed at the port 80h is the last test performed. In this case, the screen does not display the error code.

Code	Beeps	POST Routine Description
02h		Verify Real Mode
03h		Disable Non-Maskable Interrupt (NMI)
04h		Get CPU type
06h		Initialize system hardware
07h		De-shadow BIOS code
08h		Initialize chipset with initial POST values
09h		Set IN-POST flag, Verify CMOS and RTC validity

Code	Beeps	POST Routine Description
0Ah		Initialize CPU registers
0Bh		Enable CPU cache
0Ch		Initialize caches to initial POST values
0Eh		Initialize I/O component
0Fh		Initialize the local bus IDE
10h		Initialize Power Management
11h		Load alternate registers with initial POST values
12h		Restore CPU control word during warm boot
13h		Initialize PCI Bus Mastering devices
14h		Initialize keyboard controller
16h	1- 2- 2- 3	BIOS ROM checksum
17h		Initialize cache before memory autosize
18h		8254 timer initialization
1Ah		8237 DMA controller initialization
1Ch		Reset Programmable Interrupt Controller
20h	1- 3- 1- 1	Test DRAM refresh
22h	1- 3- 1- 3	Test 8742 Keyboard Controller
24h		Set ES segment register to 4 GB
26h		Enable A20 line
28h		Autosize DRAM
29h		Initialize POST Memory Manager
2Ah		Clear 512 KB base RAM
2Bh		Enhanced CMOS init
2Ch	1- 3- 4- 1	RAM failure on address line ***xxxx*** *
2Eh	1- 3- 4- 3	RAM failure on data bits ***xxxx*** * of low byte of memory bus
2Fh		Enable cache before system BIOS shadow
30h	1- 4- 1- 1	RAM failure on data bits ***xxxx*** * of high byte of memory bus
32h		Test CPU bus- clock frequency
33h		Initialize Phoenix Dispatch Manager
34h		CMOS test (on Suspend-to-Disk resume)
35h		Register re-initialization
36h		Warm start shut down
38h		Shadow system BIOS ROM
39h		Cache re-initialization
3Ah		Autosize cache
3Ch		Advanced configuration of chipset registers
3Dh		Load alternate registers with CMOS values
42h		Initialize interrupt vectors
45h		POST device initialization
46h	2- 1- 2- 3	Check ROM copyright notice
48h		Check video configuration against CMOS

Code	Beeps	POST Routine Description
49h		Initialize PCI bus and devices (I/O 81h = PCI Bus tested)
4Ah		Initialize all video adapters in system
4Bh		QuietBoot (logo) start
4Ch		Shadow video BIOS ROM
4Eh		Display BIOS copyright notice
4Fh		Multi-Boot (Boot menu support) Initialization
50h		Display CPU type and speed
51h		Initialize EISA board
52h		Test keyboard
54h		Set key click if enabled
55h		USB initialization (legacy support)
56h		Enable Keyboard
58h	2- 2- 3- 1	Test for unexpected interrupts
59h		Initialize POST display service
5Ah		Display prompt "Press DEL to enter SETUP"
5Bh		Disable CPU cache
5Ch		Test RAM between 512 and 640 KB
60h		Test extended memory
62h		Test extended memory address lines
64h		Jump to UserPatch1
66h		Configure advanced cache registers
67h		Early Initialize of Multi Processor APIC
68h		Enable external and CPU caches
69h		Setup System Management Mode (SMM) area
6Ah		Display external L2 cache size
6Bh		Load custom defaults (optional)
6Ch		Display shadow- area message
6Eh		Clear Memory
70h		Display error messages
72h		Test for configuration error detected
74h		Test RTC
76h		Check for keyboard errors
7Ch		Set up hardware interrupt vectors
7Dh		Intelligent System Monitoring initialization
7Eh		Initialize coprocessor if present
80h		Disable onboard Super I/O ports and IRQs for Auto-detection.
81h		Late POST device initialization
82h		Detect and install external RS232 ports
83h		Configure non-Motherboard Configurable Device IDE controllers
84h		Detect and install external parallel ports
85h		Initialize PC-compatible PnP ISA devices

Code	Beeps	POST Routine Description
86h		Re- initializes onboard I/O ports.
87h		Configure Motherboard Configurable Devices (optional)
88h		Initialize BIOS Data Area
89h		Enable Non-Maskable Interrupts (NMIs)
8Ah		Initialize Extended BIOS Data Area
8Bh		Test and initialize PS/2 mouse
8Ch		Initialize floppy controller
8Fh		Determine number of ATA drives (optional)
90h		Initialize hard-disk controllers, auto-detect IDE drives
91h		Initialize local-bus hard-disk controllers
92h		Jump to UserPatch2
93h		Build MPTABLE for multi-processor boards
95h		Install CD ROM for boot
96h		Clear huge ES segment register
97h		Fixup Multi Processor table
98h	1- 2	Search for option ROMs. One long, two short beeps on checksum failure
99h		Check for SMART Drive (optional)
9Ch		Set up Power Management
9Dh		Initialize security engine (optional)
9Eh		Enable hardware interrupts
9Fh		Determine number of ATA and SCSI drives (optional)
A0h		Set time of day
A4h		Initialize Typematic rate
A8h		Erase DEL prompt
AAh		Scan for DEL key stroke
ACh		Enter SETUP
AEh		Clear Boot flag
B0h		Check for errors
B2h		POST done – prepare to boot operating system
B4h	1	One short beep before boot
B5h		Terminate QuietBoot (optional)
B6h		Check password (optional)
B7h		ACPI initialization
B9h		Prepare Boot
BAh		Initialize DMI parameters
BCh		Clear parity checkers
BDh		Display MultiBoot menu
BEh		Clear screen (optional)
BFh		Display Summary Screen
C0h		Try to boot with INT 19
C1h		Initialize POST Error Manager (PEM)

Code	Beeps	POST Routine Description
C2h		Save the current boot type into CMOS
C2h		Initialize error logging
C3h		Check the requested boot type (Cold or Warm)
C3h		Initialize error display function
C4h		Initialize system error handler
C4h		Install the IRQ1 vector for BIOS Hot Keys
C5h		PnP NoteDock dual CMOS (optional)
C5h		Mark the fact that we are no longer in POST
C6h		Console Redirection SIO Initialize
C7h		Remove Console Redirection
C8h		Force Emergency Flash update check (Ctrl-E and bad CMOS)
C8h		Test Gate A20
C9h		Extended checksum (optional)
CDh		Install Console Redirection Interrupt Handler
CFh		Extended BIOS data Fail
D1h		BIOS stack initialization
D2h		Unknown interrupt
D3h		Setup WAD (reserved memory used by BIOS)
D4h		Get CPU string
E0h		Software SMI failure during POST
E1h		Memory error: Their is no memory modules
E2h		Memory error: The two memory modules type mismatch
E3h		Memory error: Memory type is not supported
E4h		Memory error: CHL Mismatch
E5h		Memory error: Size Mismatch
E8h		Memory error: Row address bits
E9h		Memory error: Internal Bank
EAh		Memory error: Timing Error
EBh		Memory error: CAS 3
ECh		Memory error: Non Registered and Registered memory have been mixed
EDh		Memory error: Case Latency not supported
EEh		Memory error: Size Not Supported
EFh		Memory error: Population order
F0h		

Code	Beeps	For Boot Block in Flash ROM
80h		Initialize the chipset
81h		Initialize the bridge
82h		Initialize the CPU
83h		Initialize system timer
84h		Initialize system I/O
85h		Check force recovery boot
86h		Checksum BIOS ROM
87h		Go to BIOS
88h		Set Huge Segment
89h		Initialize Multi Processor
8Ah		Initialize OEM special code
8Bh		Initialize PIC and DMA
8Ch		Initialize Memory type
8Dh		Initialize Memory size
8Eh		Shadow Boot Block
8Fh		System memory test
90h		Initialize interrupt vectors
91h		Initialize Run Time Clock
92h		Initialize video
93h		Initialize System Management Mode
94h	1	Output one beep before boot
95h		Boot to Mini DOS
96h		Clear Huge Segment
97h		Boot to Full DOS
A0h		Test SIO Clock Validity
A2h		Check TEST# Jumper for POST to COM, see Extension Registers.
B0h		Reset System for Erratas, Hyper-Threading
B1h		Early Boot Block Initialize completed.

E.2 POST MESSAGES

During the Power On Self Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

"PRESS F1 TO CONTINUE, DEL TO ENTER SETUP".

E.3 ERROR MESSAGES

One or more of the following messages may be displayed if the BIOS detects an error during the POST.

CMOS BATTERY HAS FAILED

1. If it is the first boot, check if the battery is installed properly
2. CMOS battery is no longer functional. It should be replaced. Consult the Intelligent System Monitoring in BIOS Setup to verify Vbat value.

CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This indicates that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

OPERATING SYSTEM NOT FOUND

No boot device was found. This could mean either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Floppy Drive A and press Enter. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

EXPANSION ROM NOT INITIALIZED

Cannot initialize the PCI expansion ROM. There is not enough free conventional memory for expansion ROM (C0000h to DFFFFh). Expansion ROM not required to boot should be disabled.

F. BIOS Update & Emergency Procedure

F.1 BIOS UPDATE PROCEDURE

The BIOS update procedure is detailed in a ReadMe file included with the BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

F.2 EMERGENCY PROCEDURE

Symptoms:

- No POST code on a power up (when using a POST card).
- Board does not boot, even after usual hardware and connection verifications.
- At power up, there is floppy disk led activity, which is one sign that the BIOS as detected a corrupted BIOS CRC prior POST and fallen back automatically to Emergency Recovery Mode looking for the floppy Emergency disk.

The Emergency Recovery procedure is detailed in a ReadMe file included with the Emergency BIOS package as well as the update utility. This package can be downloaded from our website www.kontron.com or from our FTP site ftp://ftp.kontron.ca/Support

G. Getting Help

At Kontron, we take great pride in our customers' successes. We believe in providing full support at all stages of your product development.

If at any time you encounter difficulties with your application or with any of our products, or if you simply need guidance on system setups and capabilities, contact our Technical Support at:

CANADIAN HEADQUARTERS
Tel. (450) 437-5682
Fax: (450) 437-8053

If you have any questions about Kontron, our products, or services, visit our Web site at: www.kontron.com

You also can contact us by E-mail at: support@ca.kontron.com

Or at the following address:

Kontron Canada, Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

RETURNING DEFECTIVE MERCHANDISE

Before returning any merchandise please do one of the following if your product malfunctions:

- Call

    1. Call our **Technical Support** department in Canada at **(450) 437-5682**. Make sure you have the following on hand: **our Invoice #,** your **Purchase Order #,** and the **Serial Number** of the defective unit.

    2. Provide the serial number found on the back of the unit and explain the nature of your problem to a service technician.

    3. The technician will instruct you on the return procedure if the problem cannot be solved over the telephone.

    4. Make sure you receive an **RMA #** from **our Technical Support** before returning any merchandise.

- Fax

    1. Make a copy of the request form on the following page.

    2. Fill it out.

    3. Fax it to us at: (450) 437-8053

- E-mail

    1. Send us an e-mail at: RMA@ca.kontron.com. In the e-mail, you must include your name, your company name, your address, your city, your postal/zip code, your phone number, and your e-mail. You must also include the **serial number** of the defective product and **a description of the problem.**

When returning a unit.

i) In the box, you have to include the name and telephone number of a person whom we can contact for further explanations if necessary when returning goods. **Where applicable, always include all duty papers and invoice(s) associated with the item(s) in question.**

ii) Ensure that the unit is properly packed. Pack it in a rigid cardboard box.

iii) Clearly write or mark the RMA number on the outside of the package you are returning.

iv) Ship prepaid. We take care of insuring incoming units.

Kontron Canada Inc.
616 Curé Boivin
Boisbriand, Québec
J7G 2A7 Canada

Return to Manufacturer Authorization Request

Contact Name:	_____		
Company Name:	_____		
Street Address:	_____		
City:	_____	Province/State:	_____
Country:	_____	Postal/Zip Code:	_____
Phone Number:	_____	Extension:	_____
Fax Number:	_____	E-Mail:	_____

Serial Number	Failure or Problem Description	P.O. # (if not under warranty)

Kontron Canada, Inc., 616 Curé Boivin, Boisbriand, Québec, Canada, J7G 2A7

Fax this form to Kontron's Technical Support department in Canada at (450) 437-8053